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United States Patent [19]

Matzke et al.

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[45] Date of Patent: Aug. 1, 2000

B

[54] FORMATION OF MICROCHANNELS FROM LOW-TEMPERATURE PLASMA-DEPOSITED SILICON OXYNITRIDE

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[73] Assignee: Sandia Corporation, Albuquerque, N. Mex.

[21] Appl. No.: 09/339,715

[22] Filed: Jun. 24, 1999

[51] Int. Cl.[7] H01L 21/00

[52] U.S. Cl. 438/702; 438/694; 438/698; 438/700; 205/122; 216/2; 156/643.1

[58] Field of Search 205/122; 216/2; 156/643.1; 438/694, 697, 700, 702

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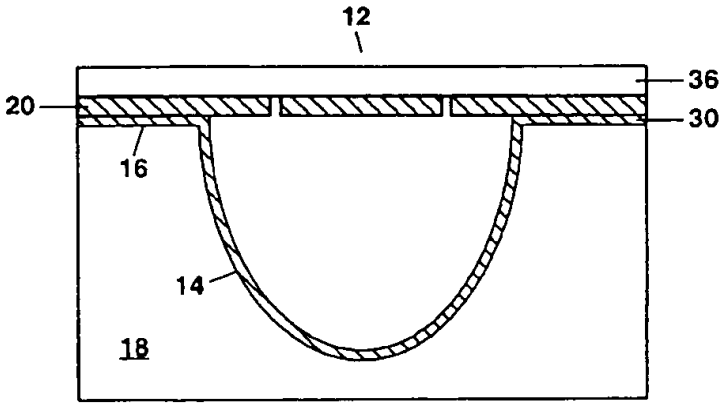
Primary Examiner—Charles Bowers
Assistant Examiner—Lisa Kilday
Attorney, Agent, or Firm—John P. Hohimer

[57] ABSTRACT

A process for forming one or more fluid microchannels on a substrate is disclosed that is compatible with the formation of integrated circuitry on the substrate. The microchannels can be formed below an upper surface of the substrate, above the upper surface, or both. The microchannels are formed by depositing a covering layer of silicon oxynitride over a mold formed of a sacrificial material such as photoresist which can later be removed. The silicon oxynitride is deposited at a low temperature (≦100° C.) and preferably near room temperature using a high-density plasma (e.g. an electron-cyclotron resonance plasma or an inductively-coupled plasma). In some embodiments of the present invention, the microchannels can be completely lined with silicon oxynitride to present a uniform material composition to a fluid therein. The present invention has applications for forming microchannels for use in chromatography and electrophoresis. Additionally, the microchannels can be used for electrokinetic pumping, or for localized or global substrate cooling.

40 Claims, 16 Drawing Sheets



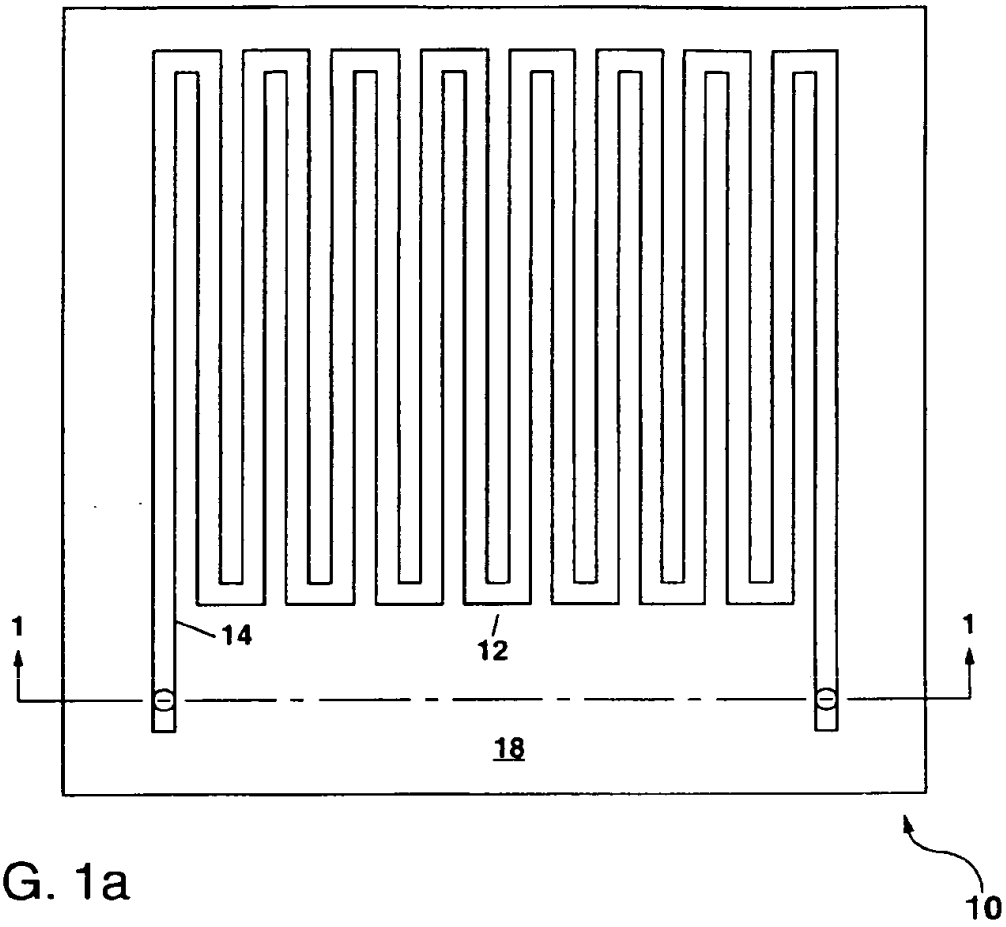
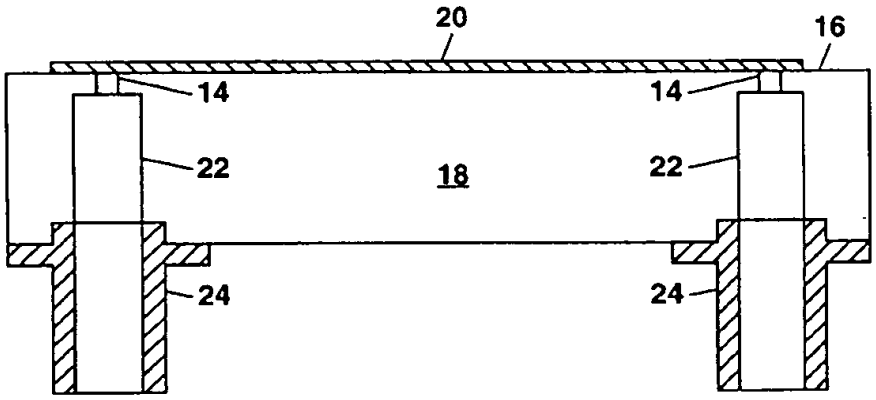


FIG. 1a



Section 1 - 1

FIG. 1b

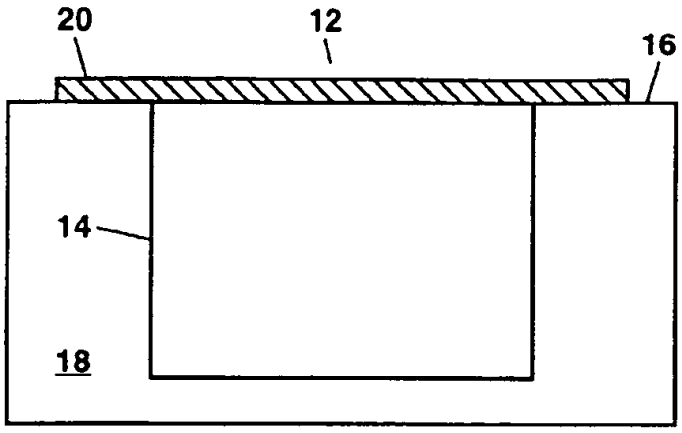


FIG. 2a

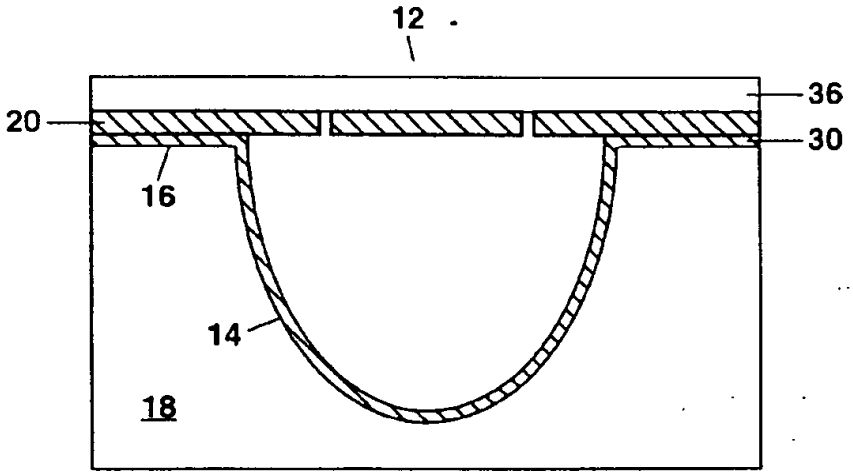


FIG. 2b

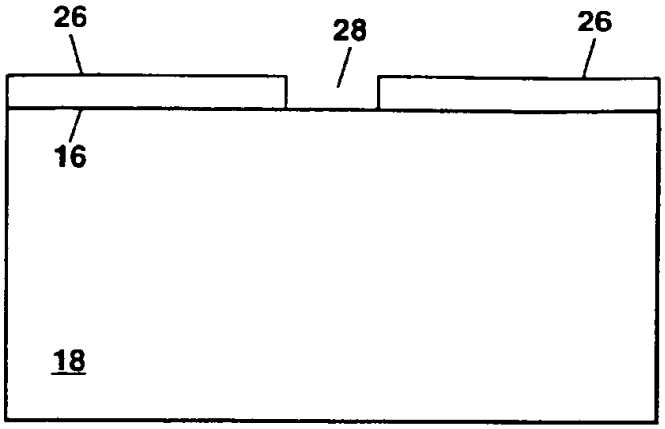


FIG. 3a

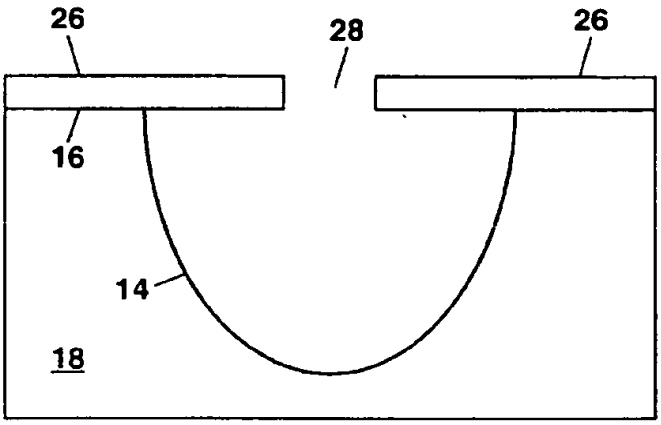


FIG. 3b

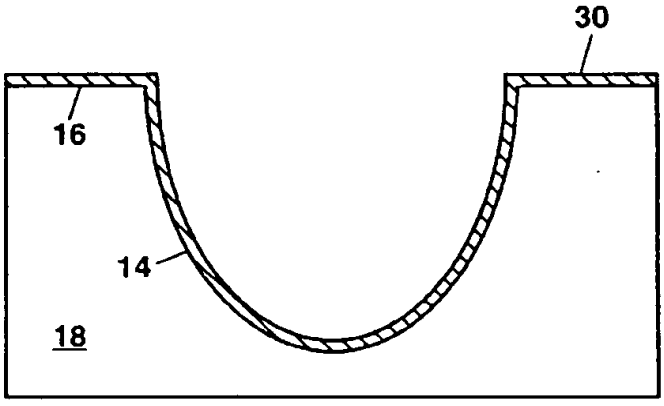


FIG. 3c

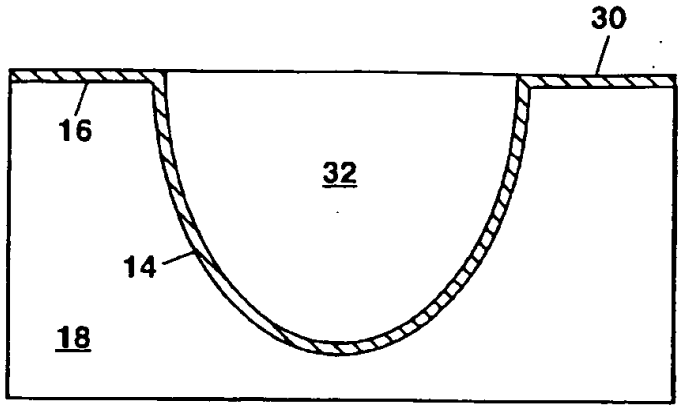


FIG. 3d

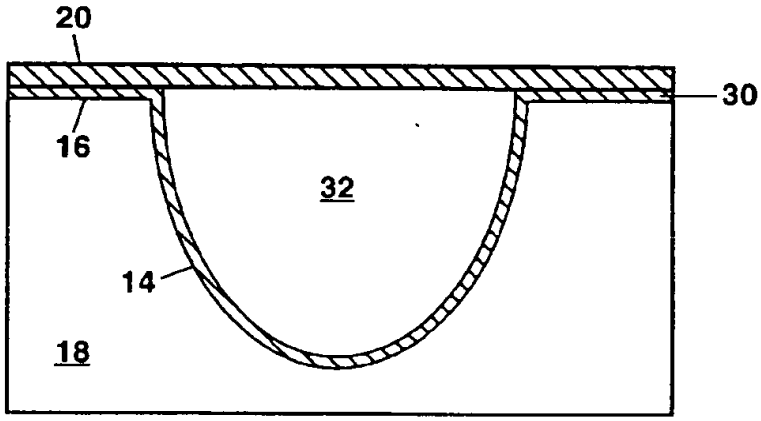


FIG. 3e

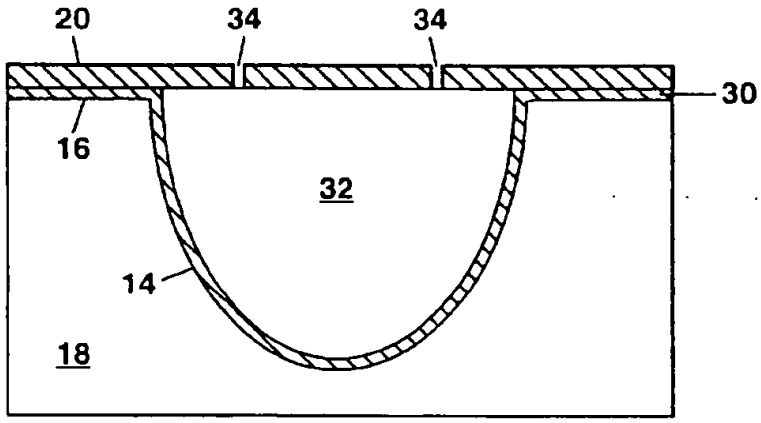


FIG. 3f

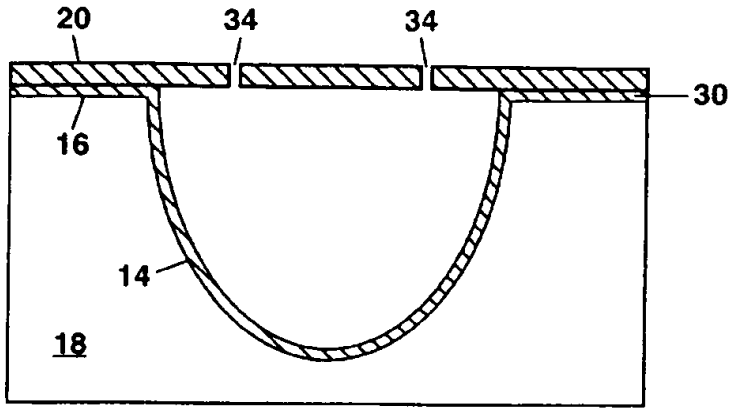


FIG. 3g

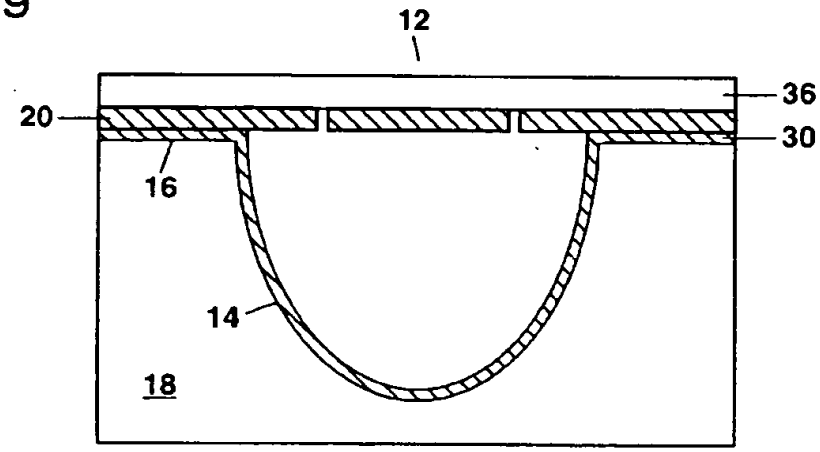


FIG. 3h

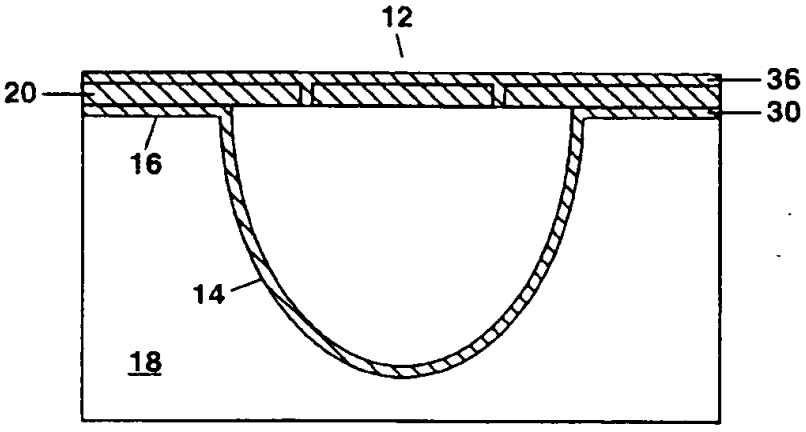


FIG. 3i

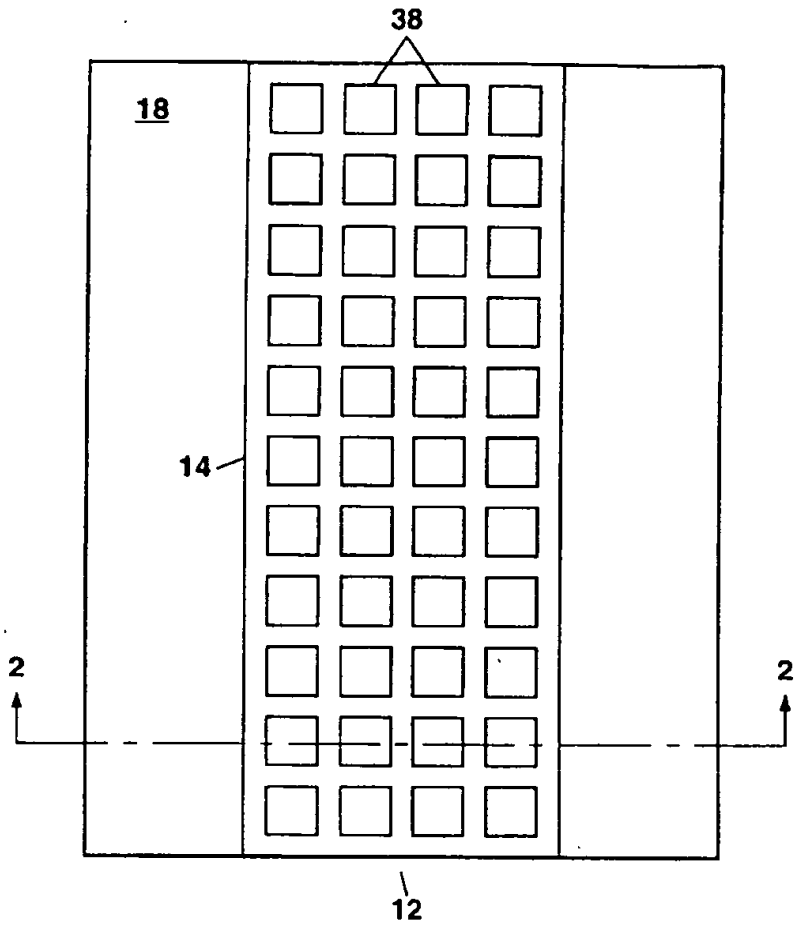
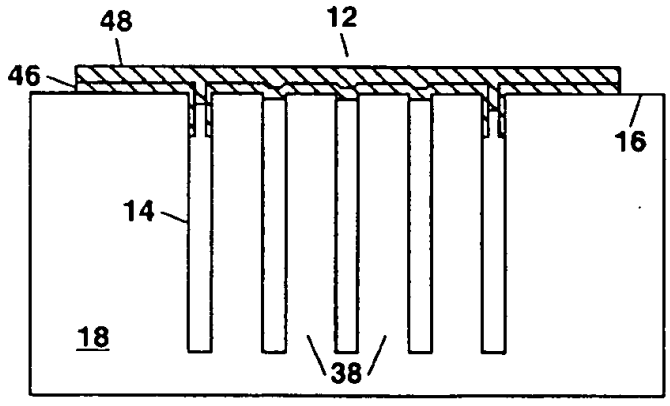


FIG. 4a



Section 2 - 2

FIG. 4b

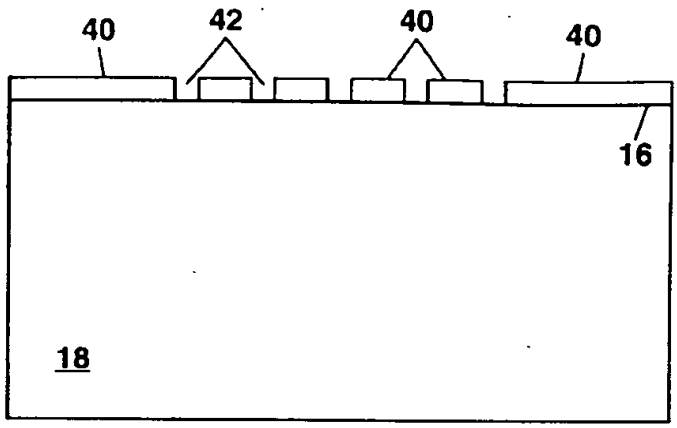


FIG. 5a

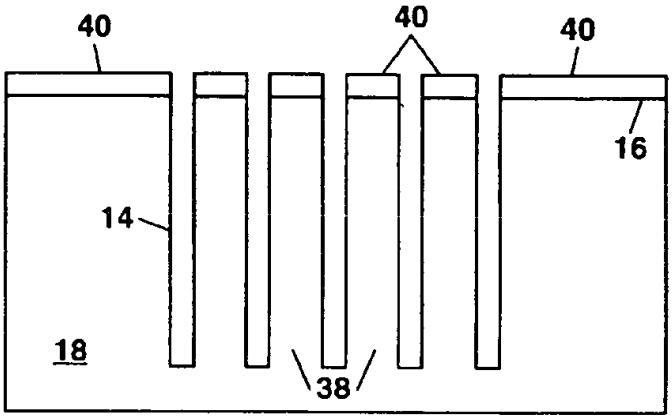


FIG. 5b

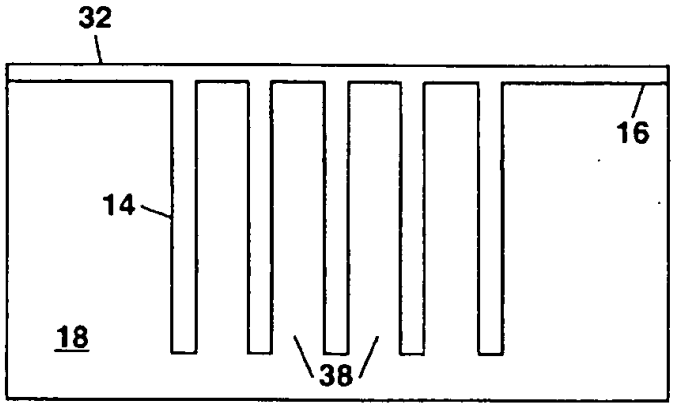


FIG. 5c

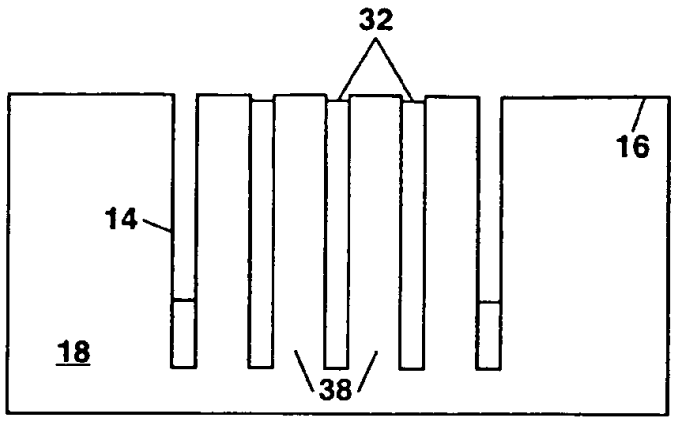


FIG. 5d

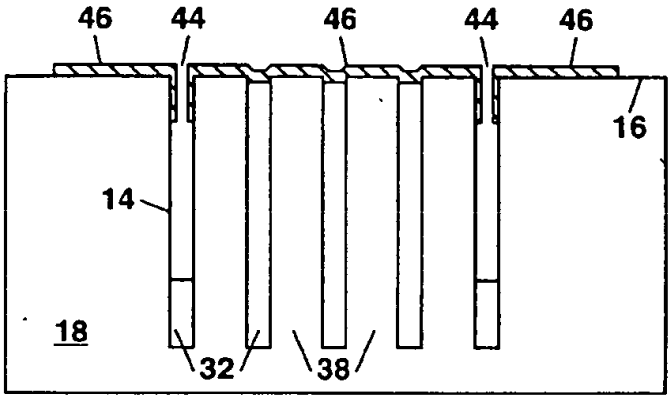


FIG. 5e

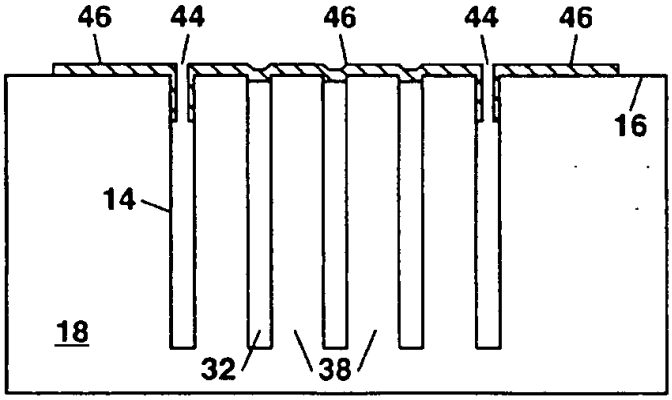


FIG. 5f

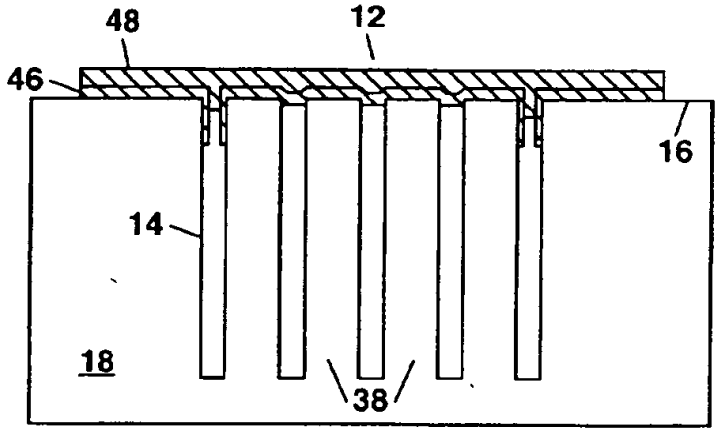


FIG. 5g

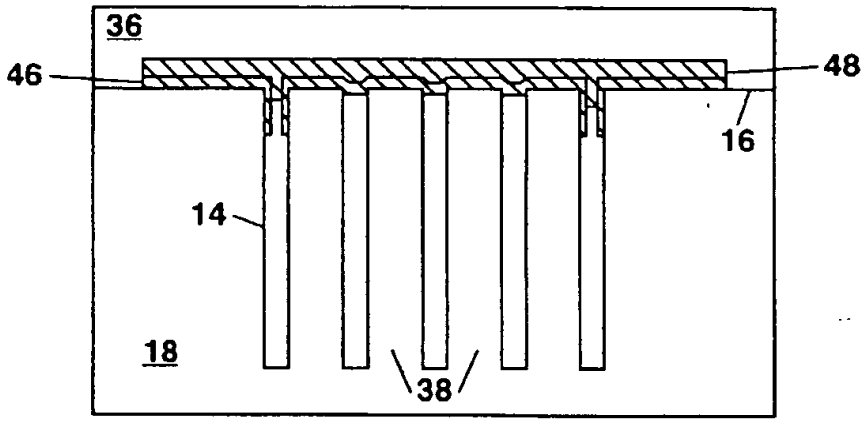


FIG. 5h

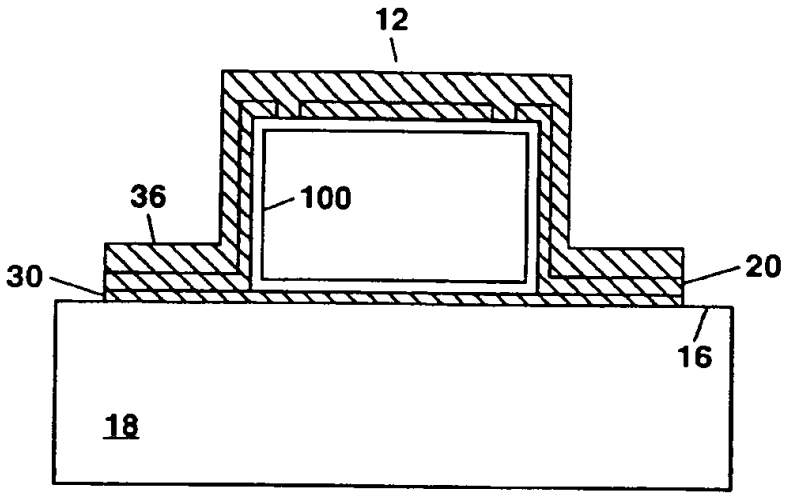


FIG. 6a

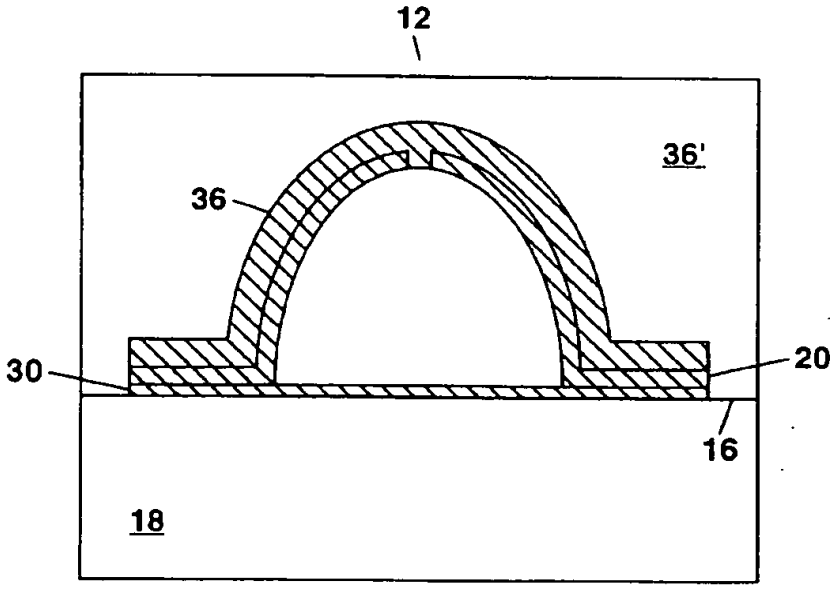


FIG. 6b

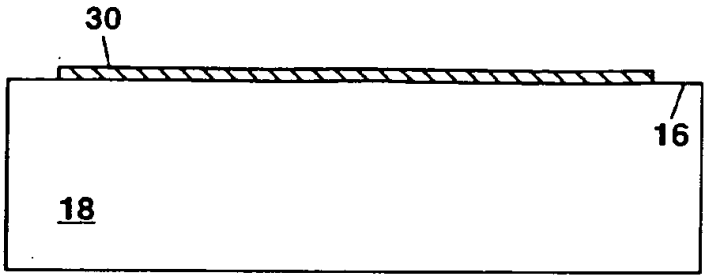


FIG. 7a

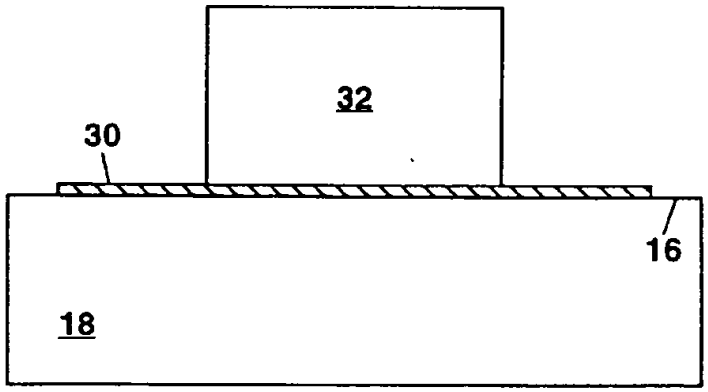


FIG. 7b

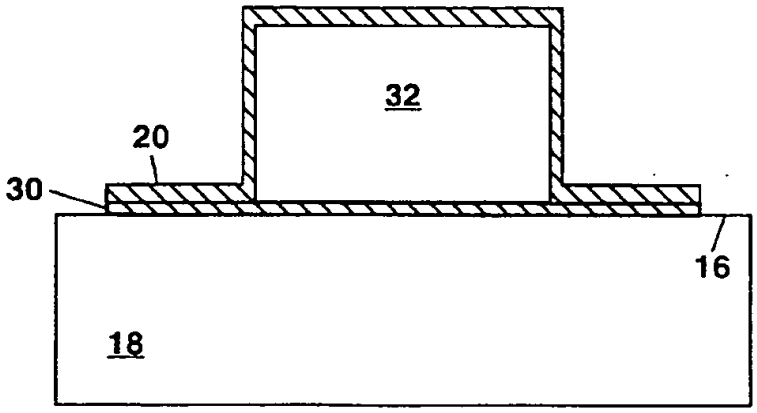


FIG. 7c

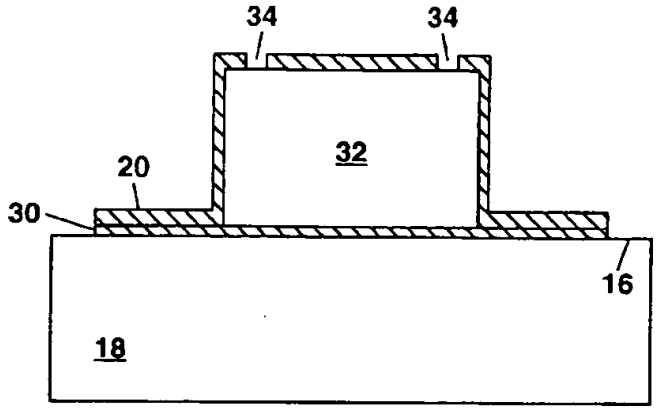


FIG. 7d

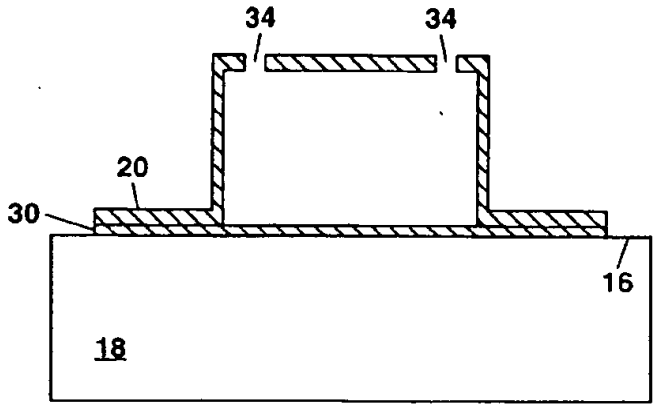


FIG. 7e

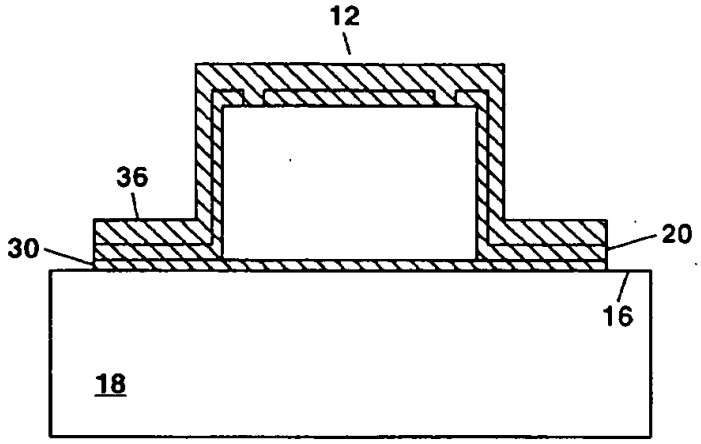


FIG. 7f

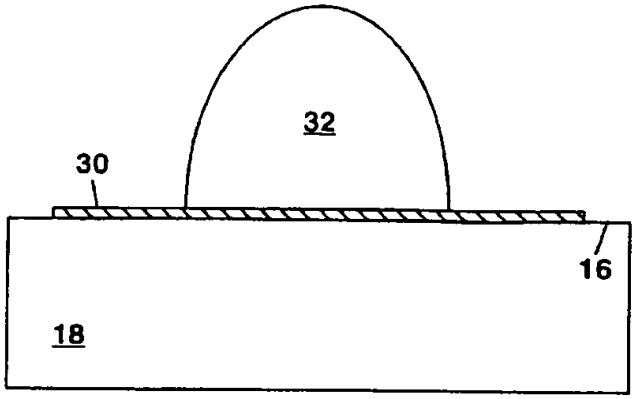


FIG. 7g

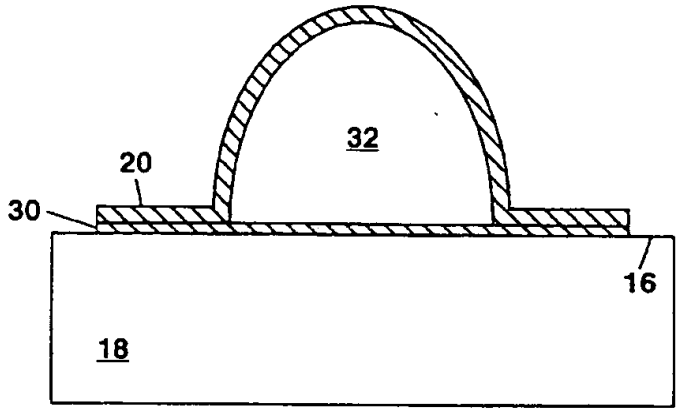


FIG. 7h

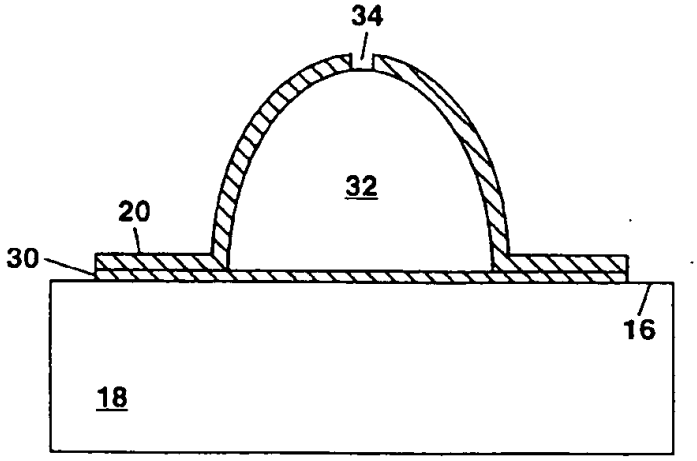


FIG. 7i

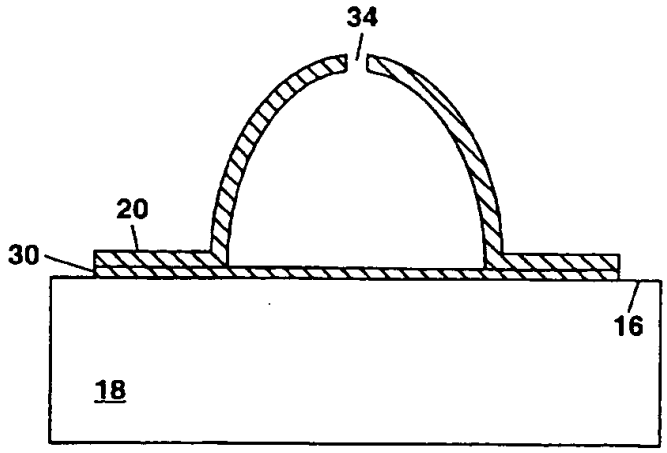


FIG. 7j

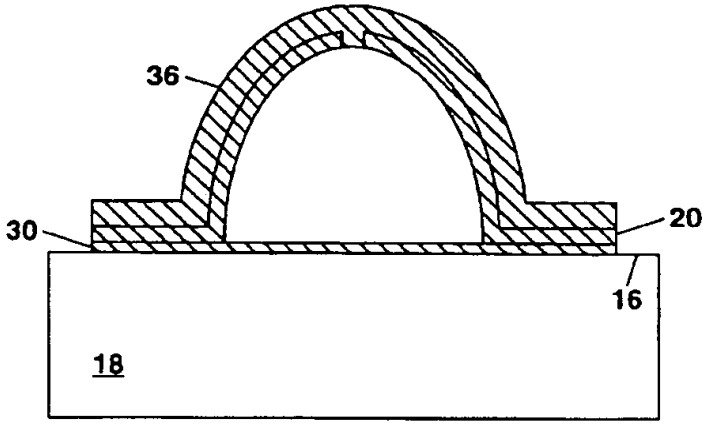


FIG. 7k

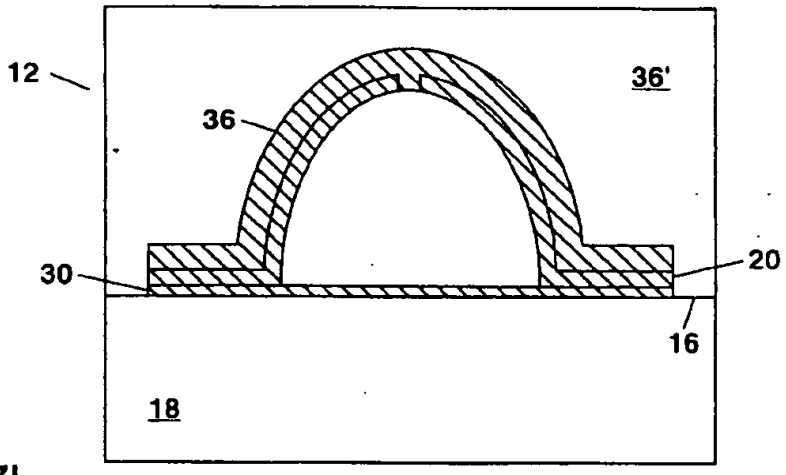


FIG. 7l

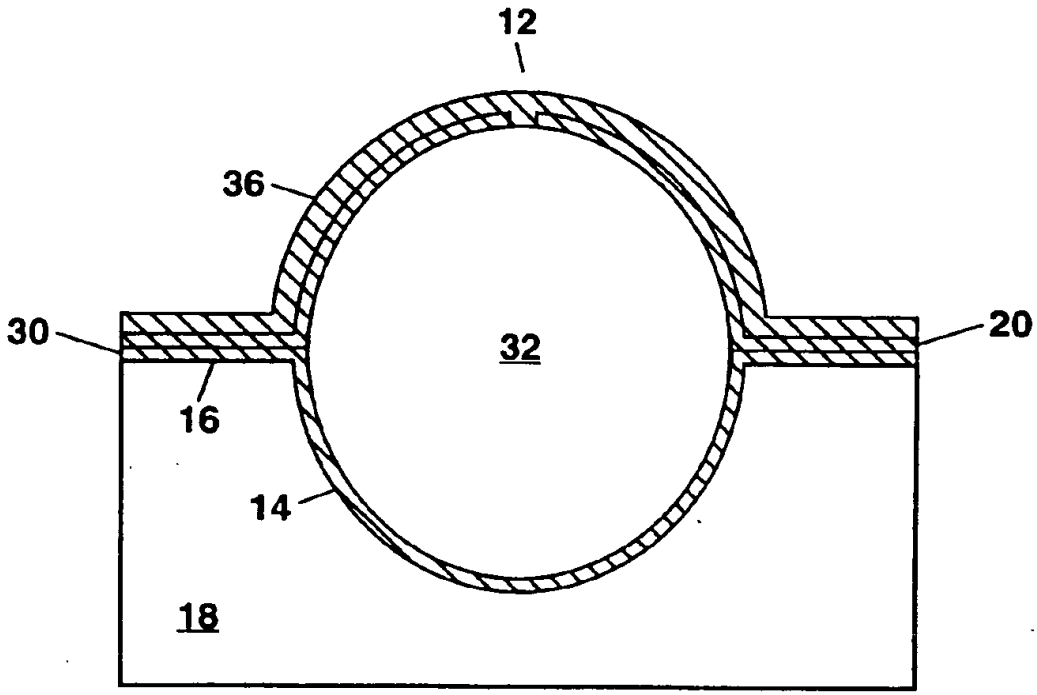


FIG. 8

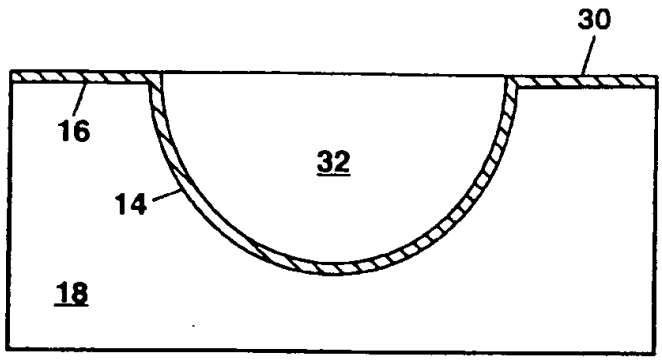


FIG. 9a

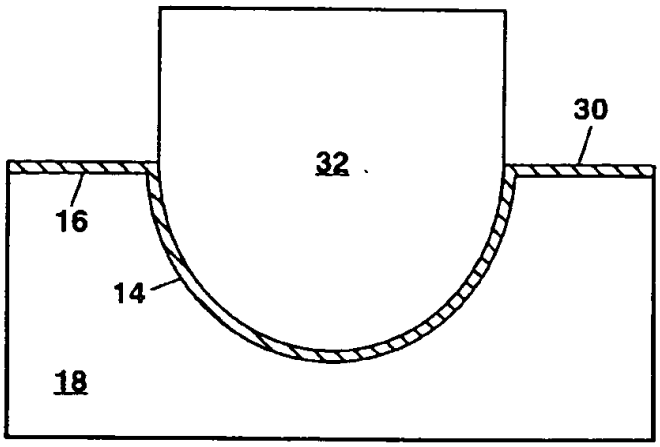


FIG. 9b

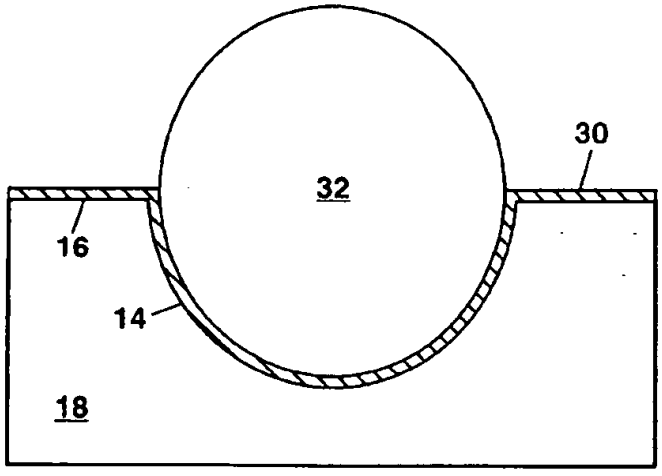


FIG. 9c

FORMATION OF MICROCHANNELS FROM LOW-TEMPERATURE PLASMA-DEPOSITED SILICON OXYNITRIDE

GOVERNMENT RIGHTS

This invention was made with Government support under Contract No. DE-AC04-94AL85000 awarded by the U.S. Department of Energy. The Government has certain rights in the invention.

FIELD OF THE INVENTION

The present invention relates generally to fluidic channels formed on or within a substrate, and specifically to a process for forming fluidic microchannels from one or more layers of silicon oxynitride deposited at a low temperature using a high-density plasma deposition process.

BACKGROUND OF THE INVENTION

The formation of one or more microchannels on or within a substrate is useful for many different types of microfluidic applications, including micro analysis systems, micromechanical actuators, localized or global substrate cooling, and ink-jet printing. Micro analysis systems which utilize miniature fluid channels include liquid and gas chromatography, electrophoresis, free-flow fractionation, and polmerase chain reaction.

Conventional methods for forming microchannels generally rely on the fabrication of the microchannels in a substrate, and then adhering or wafer bonding a cover plate over the substrate seal the microchannels (see e.g. U.S. Pat. No. 5,575,929 to Yu et al). Such conventional methods for forming microchannels can be problematic due to particulate contamination on the substrate or adhesive contamination in the microchannels. Furthermore, these conventional methods can require that the substrate be flat without any local or global warp. Finally, these conventional methods are generally not compatible with the formation of an integrated circuit on the substrate.

For many applications of microchannels, it is desirable to be able to form electronic circuitry on the same substrate as the microchannels. Such circuitry can be used to produce a flow of a particular fluid by electrokinetic pumping which can be used for separating specific components of the fluid (e.g. chromatographic or electrophoretic separation). Additionally, the provision of electronic circuitry on the substrate can be used for resistively heating the fluid, and/or for detection of specific components in the fluid for chemical analysis. Finally, electronic circuitry on the substrate can be used for signal processing, thereby forming a smart sensor.

Prior methods for forming microchannels on a substrate that are compatible with integrated circuit processing include the use of electroplated metals (see e.g. U.S. Pat. Nos. 5,871,158 and 5,876,582 to Frazier) and the deposition of various materials (e.g. silicon-carbon materials) by plasma enhanced chemical vapor deposition (see U.S. Pat. No. 5,783,452 to Jons et al).

An advantage of the present invention is that a process is disclosed whereby one or more hollow microchannels can be formed on or below a surface of a substrate, or both.

A further advantage of the present invention is that the microchannels can be fabricated using common clean-room techniques and equipment for compatibility with integrated circuit processing.

Yet another advantage of the present invention is that the microchannels can be formed at a low temperature less than 100° C. and preferably near room temperature to eliminate detrimental effects to some materials (e.g. photoresist) used in forming the microchannels. The use of low temperature processes for forming the microchannels is also advantageous for compatibility with low-melting-point substrates (e.g. polymer substrates) or for certain metallizations (e.g. aluminum) on the substrate prior to forming the microchannels.

Yet another advantage of the present invention is that the microchannels can be formed completely lined with a silicon oxynitride material to present a uniform composition surface for fluid flow, thereby eliminating possible detrimental effects due to contact of the fluid with surfaces of different compositions, or with the substrate.

Still another advantage of the present invention is that the use of silicon oxynitride to form the microchannels produces microchannels which are electrically insulating for operation at high voltages as required for electrokinetic separations.

These and other advantages of the present invention will become evident to those skilled in the art.

SUMMARY OF THE INVENTION

The present invention relates to a method for forming one or more fluid microchannels in a substrate, comprising steps for forming a trench below an upper surface of the substrate at the location of each microchannel to be formed, filling each trench with a sacrificial material; forming at least one silicon oxynitride layer covering each trench; and removing the sacrificial material from each trench to form the completed microchannel.

In some preferred embodiments of the present invention, each trench is formed by etching the substrate; whereas in other embodiments of the present invention, the trench can be formed by any method known to the art, including mechanical abrasion, molding, ion milling or laser ablation. Many different types of substrates are suitable for practice of the present invention, including semiconductors (e.g. silicon, germanium, gallium arsenide), glasses, ceramics, polymers (i.e. plastics), resins, metals (including metal alloys), ferroelectrics, crystalline quartz and fused silica. The trench formed in the substrate can be of arbitrary cross-section shape and length, with sidewalls of the trench being curved, straight (i.e. substantially perpendicular to the upper surface of the substrate) or angled. Additionally, the trench can be straight, curved, or serpentine shaped. Finally, the trench can include a plurality of shaped columns aligned substantially perpendicular to the upper surface of the substrate.

The step for filling the trench with the sacrificial material preferably comprises filling the trench with a photoresist; and the step for removing the sacrificial material preferably comprises removing the photoresist from the trench by dissolution using a solvent (e.g. acetone). To fill the trench with the photoresist, the photoresist is initially spun on over the surface of the substrate and in the trench, and then a portion of the photoresist is photolithographically exposed and developed to remove a portion of the photoresist outside the trench. Any photoresist residue remaining on the surface of the substrate can be removed with a cleaning step which preferably comprises exposing the substrate to an oxygen plasma.

Formation of the silicon oxynitride layer covering the trench is preferably performed by a high-density plasma deposition process which is carried on at a low temperature of ≦100° C., and preferably near room temperature (e.g.

20–30° C.). Many different high-density plasma deposition processes are suitable for practice of the present invention including electron-cyclotron resonance (ECR) plasma deposition and inductively-coupled plasma (ICP) deposition, but specifically excluding plasma-enhanced chemical vapor deposition (PECVD) which is a low-density plasma deposition process that proceeds at a temperature sufficiently high to lead to a polymerization of the photoresist thereby making its removal difficult. A high-density plasma deposition process is defined herein as a process carried out in a plasma containing at least 10^{11} electrons/cm^3 and generally up to about 5×10^{13} electrons/cm^3. Additionally, a high-density plasma deposition process can be defined as a plasma process which provides a positive ion flux to the surface of the substrate in the range of 1–50 mA/cm^2.

The silicon oxynitride layer can comprise a partially hydrogenated silicon oxynitride having a composition $Si_wO_xN_yH_z$, with w being in the range of 25–65 atomic percent (at. %) silicon, x being in the range of 5–40 at. % oxygen, y being in the range of 10–40 at. % nitrogen, and z being in the range of 0–25 at. % hydrogen. After removing the sacrificial material from the trench, the silicon oxynitride layer(s) can optionally be densified by a thermal annealing step, thereby strengthening the microchannel(s) and lowering the hydrogen content in the silicon oxynitride composition.

Removal of the sacrificial material from the trench can be accomplished, for example, by forming one or more openings through the silicon oxynitride layer to expose the sacrificial material which is preferably a photoresist. The photoresist can then be removed by dissolution by a solvent (e.g. acetone) with or without agitation or heating. Once the photoresist is removed, the openings through the silicon oxynitride layer can be sealed, for example, with one or more additional depositions of silicon oxynitride. Optionally, one or more encapsulating layers can be deposited over the silicon oxynitride layer(s) to further strengthen the microchannel(s) for protection, or to withstand a high internal fluid pressure.

In some embodiments of the present invention (e.g. for chromatography or electrophoresis) it is desirable that the microchannel present a uniform composition to a fluid of interest for efficient operation. This can be accomplished by lining the trench with an underlayer of silicon oxynitride prior to filling the trench with the sacrificial material. The underlayer can be formed by depositing 0.05–3 microns of silicon oxynitride over the substrate and in the trench using the high-density plasma deposition process.

The present invention further relates to a method for forming one or more fluid microchannels on a substrate by depositing a sacrificial material over an upper surface of the substrate and patterning the sacrificial material to form an elongate-shaped mold to define the microchannel being formed over the substrate, depositing at least one covering layer of silicon oxynitride over the patterned sacrificial material, and providing at least one opening for exposing the sacrificial material, and removing the sacrificial material through the opening. The same types of substrates described previously can be used to form this type of microchannel.

The sacrificial material is preferably a photoresist which is spun on over the upper surface of the substrate and patterned to form the elongate-shaped mold, with the remaining photoresist removed, and with any photoresist residue removed by a cleaning step based on exposure of the upper surface of the substrate to an oxygen plasma. The patterned photoresist can optionally be heated to a temperature sufficient to cause the photoresist to flow, thereby producing a curved cross-section shape for the mold. As described previously, the photoresist can be removed by solvent dissolution (e.g. with acetone).

The step for depositing the covering layer is preferably based on deposition of silicon oxynitride by a high-density plasma deposition process (e.g. an ECR or ICP deposition process) which proceeds at a low substrate temperature of ≦100° C., and preferably near room temperature. After removal of the sacrificial material, the covering layer can optionally be annealed to increase its density and mechanical strength.

In some embodiments of the present invention, the upper surface of the substrate can be lined with an underlayer of silicon oxynitride prior to deposition of the sacrificial material, thereby permitting the fabrication of a microchannel which presents a uniform material composition to a fluid therein. When an underlayer is used, an exposed portion of the underlayer can be treated prior to deposition of the covering layer to improve adhesion of the covering layer to the exposed portion of the underlayer.

In other embodiments of the present invention, one or more fluid microchannels can be formed which lie partially below the upper surface of the substrate and partially above the upper surface. This can be done by combining the teachings of the two methods described previously to form a trench in the substrate prior to depositing the sacrificial material to a thickness sufficient to extend upward above the surface of the substrate a predetermined distance. Once the sacrificial material (e.g. photoresist) is patterned, the resultant elongate-shaped mold will fill the trench and extend upward beyond the surface of the substrate. The mold can then be covered by depositing a covering layer (e.g. silicon oxynitride) to form the microchannel. The microchannel is completed by removing the sacrificial material (e.g. through at least one opening in the covering layer, or through at least one via-hole through the substrate that connects with the microchannel, or through one or more ends of the microchannel).

When photoresist is used as the sacrificial material, the patterned photoresist can optionally be heated and flowed to generate a curved cross-section shape for the mold. And if the trench is formed with curved sidewalls, the result can be formation of a microchannel having, for example, a circular or elliptical cross-section shape. As described previously, the trench can optionally be lined with an underlayer (e.g. silicon oxynitride) prior to deposition of the sacrificial material. Once the microchannel is formed and the sacrificial material removed, an encapsulating layer can be deposited over the covering layer, if need, to seal openings through the covering layer and/or to provide an increased mechanical strength for the microchannel.

Additional advantages and novel features of the invention will become apparent to those skilled in the art upon examination of the following detailed description thereof when considered in conjunction with the accompanying drawings. The advantages of the invention can be realized and attained by means of the instrumentalities and combinations particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated into and form a part of the specification, illustrate several aspects of the present invention and, together with the description, serve to explain the principles of the invention. The drawings are only for the purpose of illustrating preferred

embodiments of the invention and are not to be construed as limiting the invention. In the drawings:

FIG. 1*a* shows a schematic plan view of an example of a microchannel device having at least one fluid microchannel formed on a substrate according to the present invention.

FIG. 1*b* shows a schematic cross-section view along the lines 1—1 in FIG. 1*a* to illustrate how external fluid connections can be made through the substrate to the microchannel formed therein.

FIGS. 2*a* and 2*b* show schematic cross-section views of two examples of fluid microchannels that can be formed below the upper surface of the substrate according to the present invention.

FIGS. 3*a*–3*i* illustrate a series of process steps that can be used to form the microchannel of FIG. 2*b*.

FIG. 4*a* shows a schematic partial plan view of another example of a fluid microchannel that can be formed below the surface of the substrate according to the present invention prior to depositing at least two silicon oxynitride layers for sealing the microchannel; and FIG. 4*b* shows a schematic cross-section view of the microchannel of FIG. 4*a* along the lines 2—2 including the silicon oxynitride layers.

FIGS. 5*a*–5*h* illustrate a series of process steps that can be used to form the microchannel of FIGS. 4*a* and 4*b*.

FIGS. 6*a* and 6*b* show schematic cross-section views of two examples of fluid microchannels that can be formed above the upper surface of the substrate according to the present invention.

FIGS. 7*a*–7*i* illustrate a series of process steps that can be used to form the microchannels of FIGS. 6*a* and 6*b*.

FIG. 8 shows a schematic cross-section view of an example of a fluid microchannel that can be formed which extends both above and below the surface of the substrate.

FIGS. 9*a*–9*c* illustrate formation of the microchannel of FIG. 8.

DETAILED DESCRIPTION OF THE INVENTION

Referring to FIG. 1*a*, there is shown schematically in plan view an example of a microchannel device **10** that comprises a fluid microchannel **12** which can be formed according to the present invention. The microchannel **12** comprises a trench **14** formed below an upper surface **16** of a substrate **18**, with the trench **14** being covered by at least one deposited silicon oxynitride layer **20**. For clarity, the silicon oxynitride layer **20** has been omitted from FIG. 1*a*, but is shown in the cross-section view of FIG. 1*b*. As defined herein, the term "microchannel" refers to a hollow fluid duct having a width that is generally in the range from about 5 to 500 microns (μm), and a height that is generally in the same range as the width. The term "fluid" is intended to include both liquids and gases.

The microchannel **12** in the example of FIG. 1*a* has a serpentine shape to save space on the substrate **18** (e.g. for forming a compact gas or liquid chromatograph). External fluid connections (e.g. a sample injection port and an output port) can be provided to either end of the microchannel **12** as shown in FIG. 1*b* by forming via holes **22** through the lower surface of the substrate **18** to the microchannel **12** and attaching macrotubing **24** (e.g. capillary tubing) to the substrate **18**. For mechanical stability, the tubing **24** can be initially epoxied or otherwise attached to small pieces of glass having machined thru-holes to accept the tubing **24**; and then the reinforced tubing **24** can be attached to the lower surface of the substrate **18** at the via holes **22** with additional epoxy or other adhesive, or by anodic bonding. Further mechanical stabilization of the completed microchannel device **10** can be provided, if needed, by applying a strengthening material (e.g. a two-part elastomer, an epoxy, a commercial potting compound, a polyimide, or a spin-on glass) to one or both surfaces of the substrate **18**.

In the example of FIGS. 1*a* and 1*b*, the substrate **18** can comprise either a crystalline or a non-crystalline material. In particular, crystalline materials that can be used for the substrate **18** include semiconductors (e.g. silicon, germanium, gallium arsenide), crystalline quartz, and ferroelectrics (e.g. barium titanite). Non-crystalline materials that can be used as the substrate **18** can include glasses, polymers (i.e. plastics), ceramics (including ferroelectric ceramics), metals (including metal alloys), and fused silica.

Examples of microchannels **12** that can be formed extending below the surface **16** of the substrate **18** (i.e. sub-surface microchannels **12**) according to the present invention are shown schematically in the enlarged cross-section views in FIGS. 2*a* and 2*b*. FIG. 2*a* shows a microchannel **12** comprising a trench **14** having a generally rectangular cross-section shape with a pair of sidewalls aligned substantially perpendicularly to the upper surface **16** of the substrate **18**; whereas FIG. 2*b* shows a microchannel **12** formed in a trench **14** having curved sidewalls.

The exact shape for the trench **14** will depend upon the process selected to form the trench **14**, and upon the particular use for which the microchannel **12** is designed. A rectangular trench **14** for the microchannel **12** can be formed, for example, by anisotropic etching (e.g. using an anisotropic wet etchant, or an anisotropic dry etching process such as reactive ion etching), or by ion milling; whereas a trench **14** having curved sidewalls can be formed, for example, by isotropic etching, molding or laser ablation. Other cross-section shapes for the trench **14** are also possible. As an example, a trench **14** with angled sidewalls can be formed by anisotropic wet etching which stops at particular crystalline planes (e.g. {111} planes in a (100) silicon substrate **18** etched by an anisotropic wet etchant such as potassium hydroxide, tetramethyl ammonium hydroxide or ethylenediamine pyrocatechol).

In forming one or more microchannels **12** in a substrate **18** according to the present invention a series of process steps can be used as described hereinafter with reference to FIGS. 3*a*–3*i* for the case of a curved microchannel **12** as shown in FIG. 2*b*. Many of these process steps are also applicable to form the rectangular microchannel **12** of FIG. 2*a*.

A number of individual process steps are required to form the microchannel **12** of the present invention. Only the relevant process steps for the present invention will be described herein in detail since those skilled in the art understand other conventional semiconductor integrated circuit (IC) processing steps such as photolithography, masking, etching, mask stripping, and cleaning.

In FIG. 3*a*, a photoresist or metal mask **26** is formed over the substrate **18** with a slot **28** centered about a predetermined path of the microchannel **12** to be formed in the substrate **18**. The size of the slot **28** will, in general, depend upon the size of the microchannel **12** to be formed (i.e. its width and depth). A narrow slot **28** is particularly useful to form a semi-circular microchannel **12** (see U.S. Pat. No. 5,575,929 to Yu et al). As the width of the slot **28** is increased, the width of the isotropically etched microchannel **12** will increase compared to its depth. The present invention can be used to form curved microchannels **12** as shown in FIG. 2*b* having a width that is generally in the

range of about 2–500 μm and preferably about 5–100 μm, and with a depth that is up to about one-half the width.

In FIG. 3*b*, the masked substrate **18** is exposed to an isotropic wet etchant which removes material from the substrate **18** through non-preferential downward and lateral etching, thereby forming a curved trench **14** having a cross-section shape as determined by the shape of the slot **28**. Isotropic wet etchants are well known in the art for the various materials which can be used for the substrate **18**. For example, an acid mixture containing hydrofluoric acid (HF) and nitric acid (HNO_3) and either acetic acid (CH_3COOH) or water can be used to isotropically etch a silicon substrate **18**. As another example, an HF-based etchant (e.g. a buffered oxide etch) can be used to isotropically etch a glass or fused silica substrate **18**.

The present invention is not limited to forming the microchannel **12** by etching. In certain instances it can be preferable to form the microchannel **12** by other methods such as mechanical abrasion, molding (e.g. injection molding, stamping or embossing with or without heating), ion milling or laser ablation depending upon the composition of the substrate and the dimensions and dimensional tolerance required for the microchannel **12**. In such cases, the masking step of FIG. 3*a* can be omitted; and the curved trench **14** can be formed directly by one of the above processes. In the case of a plastic substrate **18**, solvent dissolution of the plastic through a patterned mask can also be used to form the trench **14**.

In FIG. 3*c*, the curved trench **14** can optionally be lined with an underlayer **30** of silicon oxynitride which can be advantageous for certain applications such as chromatography or electrophoresis. This can be done by depositing a 0.05- to 3-μm-thick layer of silicon oxynitride over the substrate **18** and in the curved trench **14** using a high-density plasma deposition process as described hereinafter.

A high-density plasma deposition process is to be distinguished from conventional capacitively-coupled radio-frequency (rf) low-density plasma systems which generally operate with electron densities in the range of 5×10^{8}–5×10^{10} cm^{-3}, with a positive ion flux of about 0.1–1 mA/cm^2. Additional input energy is generally required in a conventional rf low-density plasma; and this additional energy can be provided by heating the substrate to a temperature of about 150° C. or more. Plasma-enhanced chemical vapor deposition (PECVD) is an example of a conventional rf low-density plasma deposition system which is not suited for use in practicing the present invention.

A high-density plasma source operates at a lower pressure and lower ion energy than a conventional rf low-density plasma source, with the high-density plasma source further having a higher electron, ion and neutral radical density (i.e. an electron density of 10^{11}–5×10^{13} electrons/cm^3 and a positive ion flux of 1–50 mA/cm^2). In a high-density plasma source, the plasma generation and substrate biasing are independent or semi-independent. Since source gases are more highly dissociated in a high-density plasma, little or no substrate heating is necessary so that deposition can be carried on at a low temperature of about 100° C. or lower, and preferably at or near room temperature. This allows the use of photoresist as the sacrificial material **32**, and simplifies removal of the photoresist by solvent dissolution. At temperatures greater than 100° C. for time periods of several minutes or more, there is the possibility for polymerization of the photoresist **32** which can make its removal difficult and possibly result in damage to the microchannel **12**.

Examples of high-density plasma deposition systems which can be used to deposit the silicon oxynitride underlayer **30** in FIG. 3*c* and other silicon oxynitride layers to be described hereinafter include electron-cyclotron resonance (ECR) plasma deposition systems and inductively-coupled plasma (ICP) deposition systems. Other types of high-density plasmas systems that are also suitable for deposition of the silicon oxynitride include helicon plasma systems, multipolar plasma bucket systems, magnetron capacitively-coupled plasma systems and hollow-cathode capacitively-coupled plasma systems.

An ECR plasma deposition system uses microwaves to generate a high-density plasma from supplied source gases, and a magnetic field to keep electrons circulating in the plasma to produce a high electron density and to control beam collimation. No substrate heating is necessary for the ECR plasma deposition system; and a low substrate bias voltage of 0–100 volts. Bias voltages in the low end of the above range (e.g. about 5 volts) are to be preferred to limit etch-back of the deposited silicon oxynitride. Inductively-coupled plasma deposition systems are also referred to as transformer-coupled plasma (TCP) systems or as rf induction (RFI) systems.

To form the silicon oxynitride underlayer **30** with an ECR plasma deposition system, the ECR system can be operated at a microwave power level of generally 80–400 W, and preferably at either 125 or 385 W, with the microwave frequency generally being 2.45 GHz. Source gases which can be used to form the silicon oxynitride layer include silane (SiH_4) and one or more of a nitrogen source gas such as nitrogen (N_2), nitrous oxide (N_2O), or the combination of oxygen (O_2) and N_2. Argon (Ar) can additionally be added to the plasma.

The ECR high-density plasma can be operated at a pressure of typically 15–30 mTorr, and preferably about 20 mTorr. Flow rates for the source gases can be in the range of 5–50 standard-cubic-centimeters-per-minute (sccm) silane, 5–50 sccm of the nitrogen source gas (i.e. N_2, N_2O, or N_2+O_2), and 0–20 sccm argon. Preferred flow rates are 20 sccm silane, 30 sccm of the nitrogen source, and 4 sccm argon. A 5 volt bias is preferably provided to the substrate **18** with no substrate heating. The silicon oxynitride underlayer **30** can be deposited in the ECR plasma at a rate of 5–150 nanometers/minute, with the silicon oxynitride having a refractive index n=2.0 at a deposition rate of 20 nanometers/minute.

Under the preferred conditions above, a Rutherford backscattering measurement indicated a composition of the ECR-deposited silicon oxynitride as being 40 at. % silicon, 36 at. % nitrogen, 12 at. % oxygen and 12 at. % hydrogen. In general, the silicon oxynitride deposited according to the present invention can comprise a partially hydrogenated silicon oxynitride having a composition $Si_wO_xN_yH_z$, with w being in the range 25–65 at. % silicon, x being in the range 5–40 at. % oxygen, y being in the range 10–40 at. % nitrogen, and z being in the range 0–25 at. % hydrogen. The exact composition of the silicon oxynitride will depend upon the operating parameters of the high-density plasma deposition system, and on whether or not an annealing step is provided to densify the silicon oxynitride thereby lowering its hydrogen content. In forming the silicon oxynitride underlayer **30** with an ICP plasma source, the same source gases can be used and the flow rates and plasma parameters can be adjusted to provide a composition for the silicon oxynitride within the above range as determined from Rutherford backscattering measurements and/or index of refraction measurements.

In FIG. 3*d*, the trench **14** can be filled in with one or more layers of a sacrificial material **32**. The term "sacrificial

material" as used herein refers to a removable molding material which can be used to define inside dimensions of the microchannel **12** and later removed to leave a hollow microchannel **12** for fluid flow. The sacrificial material **32** preferably comprises photoresist (e.g. a positive tone thick photoresist) or photodefinable polymer (e.g. a photodefinable polyimide) which can be spun on over the substrate **18** in one or more layers to fill the curved trench **14**. A short spin time can be used to minimize flow of the photoresist or photodefinable polymer out of the curved trench **14**. Additionally, multiple spins and exposures may be needed to fill the trench **14** since each spun-on layer of photoresist is typically only up to 7–9 μm thick.

Photolithographic patterning and developing can be used to remove substantially all of the photoresist outside the trench **14** as shown in FIG. **3***d*. In some instances, the photoresist can extend upward beyond the upper surface **16** of the substrate. An oxygen plasma cleansing step (also termed herein a "de-scum" step) can be used to remove any photoresist residue overlying the silicon oxynitride underlayer **30** outside the trench **14**, thereby improving the adhesion of a subsequently deposited silicon oxynitride layer **20** (i.e. a covering layer) which is used to complete formation of the curved microchannel **12**.

In FIG. **3***e*, the silicon oxynitride covering layer **20** can be deposited using the same high-density plasma used previously for forming the underlayer **30**, except that the covering layer **20** is generally deposited to a greater layer thickness (e.g. about 0.5–10 μm, and preferably about 2 μm). During deposition of the silicon oxynitride covering layer **20**, it is important to keep the substrate temperature below about 90–100° C. to prevent polymerization of the photoresist **32** in the curved trench **14** which can make the photoresist **32** difficult to remove later. Preferably, the substrate **18** is maintained at or near room temperature (e.g. 20–30° C.) during deposition of the covering layer **20**.

In FIG. **3***f*, one or more shaped openings **34** (e.g. circular, rectangular, square or slotted) with a width of up to a few microns can be formed through the silicon oxynitride covering layer **20** to expose the photoresist **32** for removal by solvent dissolution using, for example, acetone. These openings **34** can be formed by masking the covering layer **20** and etching (e.g. by reactive ion etching) down through the covering layer **20** to the photoresist **32**. Alternately, the openings **34** can be formed by laser ablation.

In FIG. **3***g*, the photoresist **32** can be removed from the trench **14** by immersing the substrate **18** into a solvent such as acetone, n-methyl pyrrolidone (NMP) or a commercial photoresist stripping solution for up to several hours with or without agitation or heating. If the sacrificial material **32** comprises a photodefinable polymer, then a suitable solvent can be used to remove the polymer from the trench **14** (e.g. NMP can be used to dissolve a photodefinable polyimide). Once the sacrificial material **32** has been removed from the trench **14**, the silicon oxynitride layers **20** and **30** can optionally be densified by heating to a high temperature of 400° C. or more for about 30 seconds in a rapid thermal annealer.

In FIG. **3***h*, the openings **34** can be sealed to complete formation of the hollow microchannel **12**. This can be done by depositing an encapsulating layer **36** which can also strengthen the microchannel **12** for protection or to withstand a high internal fluid pressure. The encapsulating layer **36** can comprise, for example, a two-part elastomer (e.g. SYLGARD 184 manufactured by Dow Corning Incorporated), a photoactivated epoxy, a commercial potting compound, a polyimide or a spin-on glass. Alternately, the encapsulating layer **36** can comprise one or more metal or metal alloy layers that are deposited over the substrate by evaporation, sputtering, solution plating, or a combination thereof. The encapsulation layer **36** may or may penetrate down through the openings **34** in the covering layer **20**.

A preferred process for forming an encapsulating layer **36** using a two-part elastomer is to mix the two-part elastomer in a 10:1 ratio and de-gas the two-part elastomer in a vacuum until bubbles no longer appear in the elastomer. The two-part elastomer can then be spun onto a glass cover slip which has first been cleaned by soaking in a 1:1:5 mixture of $NH_4OH:H_2O_2:H_2O$. The elastomer is initially spun onto the glass cover slip at 500 rpm for 45 seconds to distribute the elastomer. Then the speed of the spinner is increased to 2000 rpm for another 45 seconds to form a uniform thin coating of the elastomer on the glass cover slip. The glass cover slip and elastomer coating can then be contacted to the upper surface **16** of the substrate **18** covering the openings **34**. The elastomer can be cured at either 90° C. for a few hours, or at room temperature for about 24 hours.

In some instances, the encapsulating layer **36** can comprise one or more additional silicon oxynitride layers deposited using a high-density plasma as described previously. The use of a silicon oxynitride encapsulating layer **36** can be advantageous for sealing the openings **34** through the covering layer **20** and for maintaining a uniform composition for the microchannel **12**. The use of a silicon oxynitride encapsulating layer **36** is schematically illustrated in FIG. **3***i*. Additional encapsulating layers **36** comprising, for example, a two-part elastomer can be provided over the silicon oxynitride layer **20**, if needed, for additional strength or protection.

FIG. **4***a* shows a schematic partial plan view of another type of fluid microchannel **12** that can be formed below the surface of a substrate **18** according to the present invention. The microchannel **12** is sealed with at least two deposited silicon oxynitride layers which are omitted from FIG. **4***a* for clarity. FIG. **4***b* shows a schematic cross-section view of the completed microchannel **12** of FIG. **4***a* along the lines **2**—**2** including the silicon oxynitride layers.

The microchannel **12** of FIGS. **4***a* and **4***b* includes a plurality of shaped columns **38** (also termed micro-posts) in the trench **14** arranged in an array for increasing a total surface area within the microchannel **12** (i.e. to form a packed microchannel **12**). An increased surface area can be advantageous for chromatography or electrophoresis since the separation of different chemical species can be enhanced by increasing the surface area with which the chemical species interact while traversing the microchannel **12**. This provides an increased stationary phase interaction which can reduce the length required for the microchannel **12**. Chromatographic separation of different chemical species using electrokinetic pumping is described in further detail in an article by C. M. Matzke et al entitled "Quartz Channel Fabrication for Electrokinetically Driven Separations" published in the *Proceedings of the SPIE Conference on Microfluidic Devices and Systems*, SPIE Volume 3515, pages 164–171, September 1998, which is incorporated herein by reference.

FIGS. **5***a*–**5***h* illustrate in schematic cross-section view a series of process steps that can be used to form the microchannel **12** of FIGS. **4***a* and **4***b*.

The various types of substrates **18** which can be used have been described previously. For electrokinetically driven separations, an electrically non-conductive substrate **18** is

generally required; and a preferred material for this type of substrate **18** is Z-cut crystalline quartz which etches much faster in the Z-direction than in other directions. Crystalline quartz has a further advantage in that it is optically transparent over a wide range of wavelengths so that an optical detection system (e.g. a laser or light-emitting diode and a photodetector) can be integrated with the microchannel **12** to form an electrokinetic microchannel device **10**. Therefore, the following discussion will describe formation of this embodiment of the microchannel **12** based on the use of a Z-cut crystalline quartz substrate **18**. Those skilled in the art will understand that a microchannel **12** having a plurality of shaped columns **38** therein can be formed from other types of substrates which can be anisotropically etched, including silicon substrates. For example, a (110) silicon substrate can be preferentially etched with an etchant such as potassium hydroxide, with the etchant stopping on {111} planes which are oriented perpendicular to the upper surface of the substrate.

In FIG. **5***a*, a photolithographically defined Cr/Au mask **40** is formed over the upper surface **16** of the crystalline quartz substrate **18** with a pattern **42** of openings which define the location of each microchannel **12** with the shaped columns **38** to be formed therein. To form a regular array of shaped columns **38** as shown in FIG. **4***a*, the mask **40** can be patterned to leave Cr/Au squares which define columns **38** to be formed with lateral dimensions of about 4–20 μm on a side and with a gap of about 3 μm between adjacent columns **38**, and a 3-μm-spacing between the columns **38** and the sidewalls of the trench **14**. This patterning of the Cr/Au mask **40** can be done by dry etching using argon ion milling through a photolithographically patterned photoresist mask (not shown).

In FIG. **5***b*, the crystalline quartz substrate **18** can be anisotropically etched using 49% HF with no stirring. For a given spacing between the shaped columns **38**, the measured etch depth increases as the width of each column **38** is reduced in size down to about 5 μm. Thus, etch rates appear to increase as the etchant becomes more diluted by etch reactants. An etch depth of about 40 μm can be achieved for eight hours of etching to produce a 5-cm-long serpentine microchannel **12** having a width of 80 μm, and packed with shaped columns **38** which are 5 μm on a side.

A change in shape of the columns **38** can also occur due to etching along crystalline planes so that Rrsx-facets appear due to fast etching in the Z-direction and slow etching along m-planes. This change in shape is especially pronounced as the width of the columns **38** is reduced so that the 5-μm-wide columns **38** appear substantially hexagonal in shape after etching. No substantial change in shape of the columns **38** or the gap between adjacent columns **38** occurs with increased etching depth (i.e. along the height of the columns **38**) so that after etching the shaped columns **38** and sidewalls of the trench **14** are aligned substantially perpendicular to the upper surface **16** of the substrate as shown in FIG. **5***b*.

Two-sided processing of the crystalline quartz substrate **18** can be performed to fabricate one or more packed microchannels **12** below the upper surface **16** of the substrate **18** and to form open microchannels **12** without any columns **38** on a lower surface of the substrate **18**. The two types of microchannels **12** can be interconnected with via-holes formed through the substrate **18**. The open microchannels **12** can then be connected to macrotubing tubing **24** to form sample injection and output ports.

A Cr/Au mask is used on the lower surface of the substrate **18** to define the open microchannels **12**, with the Cr/Au mask being patterned by a photoresist mask, followed by etching of the Cr/Au mask using KI/I_2 and chromium etchants. When two-sided processing of the crystalline quartz substrate **18** is used, one side can be protected during etching of the other side by a covering of a mylar sheeting or an unpatterned layer of photoresist. Once etching is complete, the Cr/Au masks can be removed from each side of the substrate **18** using the KI/I_2 and chromium etchants.

In FIG. **5***c*, a sacrificial material **32** preferably comprising photoresist can be spun on over the crystalline quartz substrate **18** to fill in the etched areas therein. The photoresist **32** can be, for example, a positive-tone thick resist which can be spun on for a short time to minimize flow of the photoresist out of the etched trench **14**.

In FIG. **5***d*, the photoresist **32** outside the trench **14** and inside the trench **14** near the sidewalls is photolithographically exposed and developed to remove this portion of the photoresist **32**. A double exposure (e.g. 8 seconds) can be used to expose the photoresist **32** to be removed within the trench **14** which can be, for example, up to 40–50 μm thick. An over-develop time of one minute can be used to aid in removal of the photoresist **32** from within the trench **14**, and also from the tops of the shaped columns **38** in a central portion of the trench **14**. The removal of the photoresist **32** near the sidewalls of the trench **14** need not be complete, but need only be removed to an extent that will allow the formation of open windows **44** in this region so that the remaining photoresist **32** can be removed by solvent dissolution.

After removal of the photoresist **32** as described above, an oxygen plasma "de-scum" step can be used to clear any photoresist residue from the tops of the shaped columns **38**, and from the upper surface **16** of the substrate **18** thereby improving adhesion of a subsequently-deposited silicon oxynitride covering layer (i.e. a first layer **46** as described hereinafter). This can result in the photoresist **32** between the shaped columns **38** being slightly recessed below the upper surface **16** of the substrate as shown in FIG. **5***d*.

In FIG. **5***e*, a first layer **46** of silicon oxynitride can be deposited over a portion of the substrate and patterned to leave the windows **44** to provide access to the trench **14**. The first layer **46** of silicon oxynitride and subsequent silicon oxynitride layers can be deposited using a high-density plasma (e.g. an ECR plasma) as described previously. For example, the thickness of the first layer **46** of silicon oxynitride can be about 350 nanometers using a 30 minute ECR deposition. At this thickness, the first layer **46** of silicon oxynitride only partially fills in the windows **44** leaving room for entry of a solvent (e.g. acetone) to dissolve away the remaining photoresist **32** as shown in FIG. **5***f*. The solvent dissolution step can proceed for several hours (e.g. 3–5 hours) as described previously.

In FIG. **5***g*, a second layer **48** of silicon oxynitride can be deposited over the substrate to fill in the windows **44**. This second layer **48** of silicon oxynitride can be, for example, about 1.2 μm thick and can be deposited from the high-density plasma at a rate of about 60 nanometers/minute. Additional layers of silicon oxynitride can be deposited, if needed, to completely fill in the windows **44** to form a hollow microchannel **12**. An annealing step can optionally be provided to densify the silicon oxynitride layers **46** and **48** after removal of the photoresist sacrificial material **32**.

In FIG. **5***h*, an encapsulating layer **36** as described previously (e.g. comprising a two-part elastomer, an epoxy, a commercial potting compound, a polyimide, or a spin-on glass) can also be provided over the microchannel **12** if

needed for protection or for strengthening the microchannel 12 to withstand higher internal fluid pressures. In some embodiments of the present invention, the encapsulating layer 36 can be substituted for the second layer 48 of silicon oxynitride to simplify processing and reduce manufacturing cost.

After formation, the microchannel 12 can be coated inside with a stationary phase coating material 100 as used in the art of chromatography or electrophoresis (see FIG. 6a). Commonly used stationary phase coating materials 100 consist of polymers synthesized with specific chemical groups with the proper physico-chemical interactions to cause separation of a chemical species of interest from a gaseous or liquid sample to be analyzed. Different methods can be used to coat the microchannel 12 of FIGS. 4a and 4b with a particular stationary phase coating material 100. For example, this can be done by pushing a plug of a selected stationary phase coating material 100 (e.g. a long-chain hydrocarbon based on silane chemistry) through the microchannel 12 using pressurized gas. Alternately, the microchannel 12 can be filled with the stationary phase coating material 100; and then the excess material 100 can be removed from the microchannel 12 by applying a vacuum at one end of the microchannel 12 (e.g. via macrotubing 24).

Electrodes can be formed spaced along the microchannel 12 for electrokinetic pumping. This can be done by forming openings to the interior of the microchannel 12 and depositing a chemically-resistant metal (e.g. platinum or gold) to form the electrodes. Alternately, the electrodes can be formed by depositing metal at within the microchannel 12 prior to deposition of the silicon oxynitride layers 46 and 48. In some cases, the electrodes can be formed in fluid reservoirs connected to the microchannel 12.

According to the present invention, one or more microchannels 12 can also be formed above an upper surface 16 of a substrate 18 (i.e. to form above-surface microchannels 12). FIGS. 6a and 6b illustrate in cross-section view examples of microchannels 12 that can be formed above a substrate 18 according to the present invention. FIG. 6a shows an example of a microchannel 12 formed above the substrate 18 with a rectangular or square cross-section; and FIG. 6b shows an example of a curved microchannel 12. The formation of these types of microchannels 12 can be understood with reference to FIGS. 7a-7.

In FIG. 7a, a substrate 18 can be initially prepared for formation of the microchannel 12 by depositing a silicon oxynitride underlayer 30 on a portion of the upper surface 16 of the substrate 18. The substrate 18 can comprise any of the materials described previously, including semiconductors, crystalline quartz, fused silica, glasses, ceramics, polymers, metals and ferroelectrics.

In FIG. 7a, the underlayer 30, which has a composition in the range previously described and a layer thickness from 0.05 μm to 3 μm, allows formation of the microchannel 12 that is completely lined with silicon oxynitride to present a uniform composition surface for fluid flow, thereby eliminating possible detrimental effects due to contact of the fluid with surfaces of different compositions, or to prevent a chemical reaction with the substrate 18. Deposition of the silicon oxynitride underlayer 30 can be performed using a high-density plasma as described previously. The underlayer 30 can also serve to electrically insulate the microchannel 12 and fluid therein from an electrically-conducting substrate 18 (e.g. for electrokinetic pumping of the fluid). In some embodiments of the present invention, the process step of FIG. 7a can be omitted when it is not essential to have a uniform-composition microchannel 12.

In FIG. 7b, one or more layers of a sacrificial material 32 are deposited over the substrate 18 and are photolithographically patterned to leave an elongate-shaped mold for defining the dimensions of the microchannel 12 being formed. The sacrificial material 32 preferably comprises photoresist. After forming the mold as shown in FIG. 7b, an oxygen plasma "de-scum" step can be used as described previously to remove any photoresist residue from exposed portions of the silicon oxynitride underlayer 30 not covered by the mold. The oxygen plasma "de-scum" step can be limited in time duration to prevent substantial erosion of the photoresist 32 which forms the mold.

In FIG. 7c, a silicon oxynitride covering layer 20 is deposited over the mold (i.e. over the photoresist 32) and over the exposed portions of the underlayer 30 using the high-density plasma. During this step, the substrate 18 is maintained at a temperature of ≦100° C. and preferably near room temperature (e.g. 20–30° C.). The thickness of the covering layer 20 can be in the range of 0.5–10 μm and preferably about 2 μm, with a composition similar to that of the underlayer 30.

In FIG. 7d, one or more openings 34 can be formed through the covering layer 20 to expose the photoresist 32 for removal by solvent dissolution. The openings 34, which can have an arbitrary shape (e.g. a plurality of micron-sized holes, or one or more slots), can be formed by etching (e.g. reactive ion etching) using a photolithographically defined mask, or alternatively by laser ablation. In some instances, the photoresist 32 can be removed through an open end of the microchannel 12, even though the microchannel 12 can have a length of many centimeters. For example, removal of the photoresist 32 from the open ends of a serpentine microchannel that is 28-centimeters long, 80-μm wide and 30-μm high can be accomplished in a reasonable time of 2–3 hours.

Removal of the photoresist 32 by solvent dissolution can also be performed through one or more via-holes 22 formed through the substrate 18 and connected with the microchannel 12 (see FIG. 1b). Such via-holes 22 through the substrate 18 (e.g. a silicon substrate) can be formed, for example, by using a deep reactive ion etching process which combines multiple anisotropic etching steps with steps for simultaneously depositing an isotropic polymer / inhibitor to minimize lateral etching as disclosed in U.S. Pat. No. 5,501,893 to Laermer et al. In some cases, it will be preferable to form the via-holes 22 prior to forming the microchannel 12. If this is done, a photoresist 32 can be selected with an appropriate viscosity which will allow the photoresist 32 to cover the via-holes 22 during formation of the microchannel 12.

In FIG. 7e, the photoresist 32 is removed from the microchannel 12 being formed by placing the substrate 18 in a solvent bath (e.g. acetone) with or without agitation and/or heating. The solvent enters the microchannel 12 through the openings 34 and dissolves away the photoresist 32. This process can take several hours.

In FIG. 7f, the openings 34 can be sealed with an encapsulating layer 36 as described previously with reference to FIGS. 3h and 3i. To form a microchannel 12 that is completely lined with silicon oxynitride, the encapsulating layer 36 can comprise another layer of silicon oxynitride deposited using the high-density plasma as described previously. This silicon oxynitride encapsulating layer 36 preferably has a composition that is substantially the same as the layers 20 and 30, and has a layer thickness which is generally in the range of 0.5–10 μm. The exact thickness of the silicon oxynitride encapsulating layer 36 will depend on

the size of the openings 34 to be sealed, and also on the strength needed for the microchannel 12.

This completes formation of the microchannel 12. For chromatographic applications, the interior of the microchannel 12 can be coated with a stationary phase coating material 100 as shown in FIG. 6*a* and as previously described with reference to FIG. 5*h*.

To form a curved microchannel 12 above the upper surface 16 of the substrate 18, the steps described hereinafter with reference to FIGS. 7*g*–7*i* can be performed after the steps of FIGS. 7*a* and 7*b*.

In FIG. 7*g*, the photoresist 32 which forms the mold for the microchannel 12 to be formed can be heated to above a reflow temperature (i.e. to a temperature generally in the range of 80–140° C., and preferably about 130° C.) for sufficient time (i.e. from a few seconds to about 20 seconds) so that surface tension will cause the photoresist 32 to flow, thereby rounding the exposed sides and edges of the photoresist 32 to form a curved mold. The exact cross-section shape of the curved mold (e.g. semi-circular or semi-elliptical) will depend on the width and height of the photoresist 32 and the temperature used to soften or flow the photoresist 32.

Further processing to form the curved microchannel 12 as shown in FIGS. 7*h*–7*k* can proceed as described with reference to FIGS. 7*c*–7*f*. In FIG. 7*i*, an optional second encapsulating layer 36' can be provided for local or global substrate planarization or to further increase the strength of the curved microchannel 12. The second encapsulating layer 36' can comprise a two-part elastomer, an epoxy, a potting compound, a polyimide, a spin-on glass or the like. If a thermal annealing step is used to densify the various silicon oxynitride layers, this step is preferably performed before application of the second encapsulating layer 36'.

The types of above-surface microchannels 12 shown in FIGS. 6*a* and 6*b* can be combined with the sub-surface microchannels 12 of FIGS. 2*a* and 2*b* or FIGS. 4*a* and 4*b* to form a microchannel device 10 with multiple interconnecting or crossing microchannels (i.e. a network of microchannels 12). Furthermore, additional levels of microchannels 12 can be formed with or without planarizing each underlying level of microchannels 12 (e.g. by an encapsulating layer 36' as shown in FIG. 7*i*).

The teachings of the present invention for forming above-surface and sub-surface microchannels 12 can also be combined as shown in FIG. 8 to form a microchannel 12 which lies partially below the upper surface 16 of the substrate 18, and partially above the surface 16. FIGS. 9*a*–9*f* schematically illustrate the formation of a microchannel 12 having a curved cross-section shape (e.g. circular or elliptical) by combining some of the process steps used to form the curved sub-surface microchannel 12 of FIG. 2*b* with additional process steps used to form the curved above-surface microchannel 12 of FIG. 6*b*.

In FIG. 9*a*, a trench 14 is lined with a silicon oxynitride underlayer 30 and then filled with photoresist 32 as previously described with reference to FIGS. 3*a*–3*d*.

In FIG. 9*b*, one or more additional layers of photoresist 32 are spun on over the substrate 18 and patterned as shown to form an elongate-shaped mold extending upward from the upper surface 16 of the substrate 18 as described with reference to FIG. 7*b*.

In FIG. 9*c*, the substrate 18 is heated to flow the photoresist 32 as described with reference to FIG. 7*g*, thereby rounding the portion of the photoresist 32 extending upward beyond the upper surface 16 of the substrate 18. Further processing can then proceed to form the microchannel 12 with a curved cross-section shape following the process steps outlined with reference to FIGS. 7*h*–7*k*.

The process described herein for fabricating one or more microchannels 12 on a substrate 18 is compatible with standard integrated circuit processing so that integrated circuitry can be formed on the upper surface 16 of the substrate 18 prior to the formation of the microchannels 12. This allows the formation of electrodes which can penetrate into the microchannels 12 or reservoirs connected thereto for electrokinetic pumping of fluids. Additionally, electronic circuitry can be fabricated on the substrate 12 to process analytical signals derived using one or more microchannels 12, or to control operation of a microchannel device 10.

The microchannels 12 formed according to the present invention also have non-analytical applications. For example, one or more microchannels 12 can be formed on a front side or on a backside of an integrated circuit for localized or global substrate cooling. Localized front-side cooling of critical heat-producing circuit elements (e.g. power or output transistors) can be achieved by forming one or more microchannels 12 above or proximate to the heat-producing elements to cool the elements via a circulating fluid coolant.

The matter set forth in the foregoing description and accompanying drawings is offered by way of illustration only and not as a limitation. Other applications and variations of the present invention will become evident to those skilled in the art. The actual scope of the invention is intended to be defined in the following claims when viewed in their proper perspective based on the prior art.

What is claimed is:

1. A method for forming a fluid microchannel in a substrate, comprising steps for:

(a) forming a trench below an upper surface of the substrate;

(b) filling the trench with a sacrificial material;

(c) forming at least one silicon oxynitride layer covering the trench; and

(d) removing the sacrificial material from the trench, thereby forming the microchannel.

2. The method of claim 1 wherein the step for forming the trench comprises forming the trench by etching.

3. The method of claim 2 wherein the step for forming the trench comprises etching the trench in a substrate selected from the group consisting of semiconductors, crystalline quartz, fused silica, glasses, ceramics, polymers, metals, and ferroelectrics.

4. The method of claim 1 wherein the step for forming the trench comprises forming the trench with a pair of sidewalls aligned substantially perpendicular to the upper surface of the substrate.

5. The method of claim 4 wherein the step for forming the trench further comprises forming a plurality of shaped columns in the trench, with the shaped columns being aligned substantially perpendicular to the upper surface of the substrate.

6. The method of claim 1 wherein the step for forming the trench comprises forming the trench with curved sidewalls.

7. The method of claim 1 wherein the step for filling the trench with the sacrificial material comprises spinning on a photoresist or photodefinable polymer over the surface of the substrate and in the trench, photolithographically exposing and developing the photoresist or photodefinable polymer to remove a portion thereof outside of the trench.

8. The method of claim 7 wherein the step for removing the sacrificial material comprises removing the photoresist

or photodefinable polymer from the trench by dissolution using a solvent.

9. The method of claim 1 further including a step for cleaning the substrate to remove any sacrificial material from the upper surface of the substrate after the step for filling the trench with the sacrificial material.

10. The method of claim 9 wherein the step for cleaning the substrate comprises exposing the substrate to an oxygen plasma for sufficient time to remove the sacrificial material from the upper surface of the substrate.

11. The method of claim 1 wherein the step for depositing the silicon oxynitride layer comprises depositing the silicon oxynitride layer by a high-density plasma deposition process.

12. The method of claim 11 wherein the step for depositing the silicon oxynitride layer is carried on at a substrate temperature of ≦100° C.

13. The method of claim 11 wherein the high-density plasma deposition process comprises electron-cyclotron resonance (ECR) plasma deposition or inductively-coupled plasma (ICP) deposition.

14. The method of claim 13 wherein the silicon oxynitride after deposition thereof has a composition $Si_wO_xN_yH_z$, with 25–65 atomic percent (at. %) silicon (Si), 5–40 at. % oxygen (O), 10–40 at. % nitrogen (N), and 0–25 at. % hydrogen (H).

15. The method of claim 14 further including a step for densifying the silicon oxynitride by thermal annealing after the step for removing the sacrificial material from the trench.

16. The method of claim 1 further including a step for lining the trench with an underlayer of silicon oxynitride prior to the step for filling the trench with the sacrificial material.

17. The method of claim 16 wherein the underlayer has a thickness in the range of 0.05 microns.

18. The method of claim 1 wherein the step for removing the sacrificial material from the trench comprises forming at least one opening through the silicon oxynitride layer to expose the sacrificial material.

19. The method of claim 18 further including a step for sealing each opening through the silicon oxynitride layer after the step for removing the sacrificial material from the trench.

20. The method of claim 1 further including a step for depositing an encapsulating layer over the silicon oxynitride layer after the step for removing the sacrificial material.

21. A method for forming a fluid microchannel on a substrate, comprising steps for:

(a) depositing a sacrificial material over an upper surface of the substrate and patterning the sacrificial material to form an elongate-shaped mold for the microchannel to be formed on the substrate;

(b) depositing at least one covering layer of silicon oxynitride over the patterned sacrificial material, and providing at least one opening for exposing the sacrificial material; and

(c) removing the sacrificial material through the opening, thereby forming the microchannel.

22. The method of claim 21 wherein the substrate comprises a material selected from the group consisting of semiconductors, crystalline quartz, fused silica, glasses, ceramics, polymers, metals, and ferroelectrics.

23. The method of claim 21 wherein the step for depositing the sacrificial material comprises spinning on a photoresist over the upper surface of the substrate, and patterning the photoresist to form the mold.

24. The method of claim 23 further including a step for heating the patterned photoresist and flowing the patterned photoresist, thereby producing a curved cross-section shape for the mold.

25. The method of claim 23 wherein the step for removing the sacrificial material comprises removing the photoresist by solvent dissolution.

26. The method of claim 23 further including a step for cleaning the upper surface of the substrate to remove any photoresist residue after patterning of the photoresist by exposing the upper surface of the substrate to an oxygen plasma for sufficient time to remove the photoresist residue.

27. The method of claim 21 wherein the step for depositing the covering layer comprises depositing the covering layer by a high-density plasma deposition process.

28. The method of claim 27 wherein the high-density plasma deposition process is carried on at a substrate temperature of ≦100° C.

29. The method of claim 27 wherein the high-density plasma deposition process comprises electron-cyclotron resonance (ECR) plasma deposition or inductively-coupled plasma (ICP) deposition.

30. The method of claim 21 wherein the silicon oxynitride covering layer after deposition thereof has a composition $Si_wO_xN_yH_z$, with 25–65 atomic percent (at. %) silicon (Si), 5–40 at. % oxygen (O), 10–40 at. % nitrogen (N), and 0–25 at. % hydrogen (H).

31. The method of claim 30 further including a step for densifying the silicon oxynitride covering layer by thermal annealing after the step for removing the sacrificial material.

32. The method of claim 21 further including a step for lining the upper surface of the substrate with an underlayer of silicon oxynitride layer prior to the step for depositing the sacrificial material.

33. The method of claim 32 further including a step for treating an exposed portion of the underlayer prior to the step for depositing the covering layer to improve adhesion of the covering layer to the exposed portion of the underlayer.

34. The method of claim 21 further including a step for forming a trench in the substrate prior to the step for depositing the sacrificial material.

35. The method of claim 34 further including a step for lining the trench with an underlayer of silicon oxynitride layer prior to the step for depositing the sacrificial material.

36. The method of claim 34 wherein the step for depositing the sacrificial material over the substrate fills the trench, with the sacrificial material extending upward beyond the upper surface of the substrate.

37. The method of claim 35 wherein the mold formed by patterning the sacrificial material lies within the trench and further extends upward beyond the upper surface of the substrate.

38. The method of claim 36 wherein the sacrificial material comprises a photoresist, and further including a step, after patterning of the photoresist to form the mold, for heating the photoresist to a temperature sufficiently high to produce a flowing of the photoresist, thereby generating a curved cross-section shape for the mold.

39. The method of claim 21 further including a step for sealing each opening after the step for removing the sacrificial material.

40. The method of claim 21 further including a step for depositing an encapsulating layer over the covering layer after the step for removing the sacrificial material.

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(54) **INDUCTIVELY COUPLED PLASMA CVD**

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(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Under 35 U.S.C. 154(b), the term of this patent shall be extended for 0 days.

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(52) **U.S. Cl.** **438/788**; 438/624; 438/631; 438/695; 438/784; 438/786; 438/778; 438/788; 438/789; 438/902; 438/906; 427/573; 427/579; 204/192.23

(58) **Field of Search** 438/695, 788, 438/789, 631, 786, 778, 902, 784, 906, 624; 427/573, 579; 204/192.23

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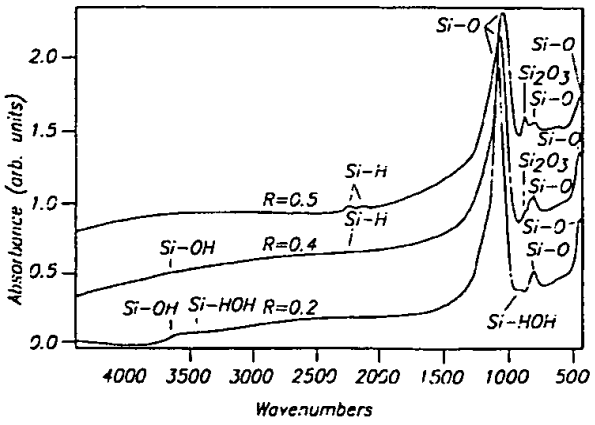
(57) **ABSTRACT**

A method of depositing a dielectric film on a substrate in a process chamber of an inductively coupled plasma-enhanced chemical vapor deposition reactor. Gap filling between electrically conductive lines on a semiconductor substrate and depositing a cap layer are achieved. Films having significantly improved physical characteristics including reduced film stress are produced by heating the substrate holder on which the substrate is positioned in the process chamber.

60 Claims, 4 Drawing Sheets



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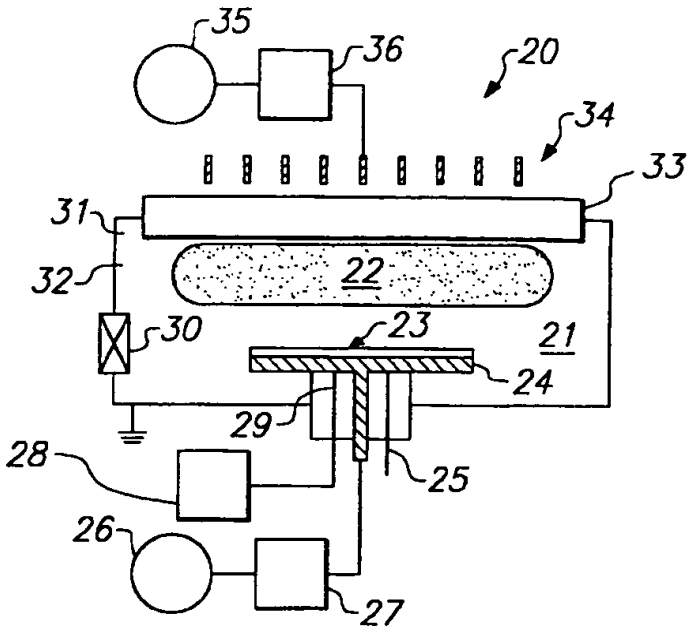
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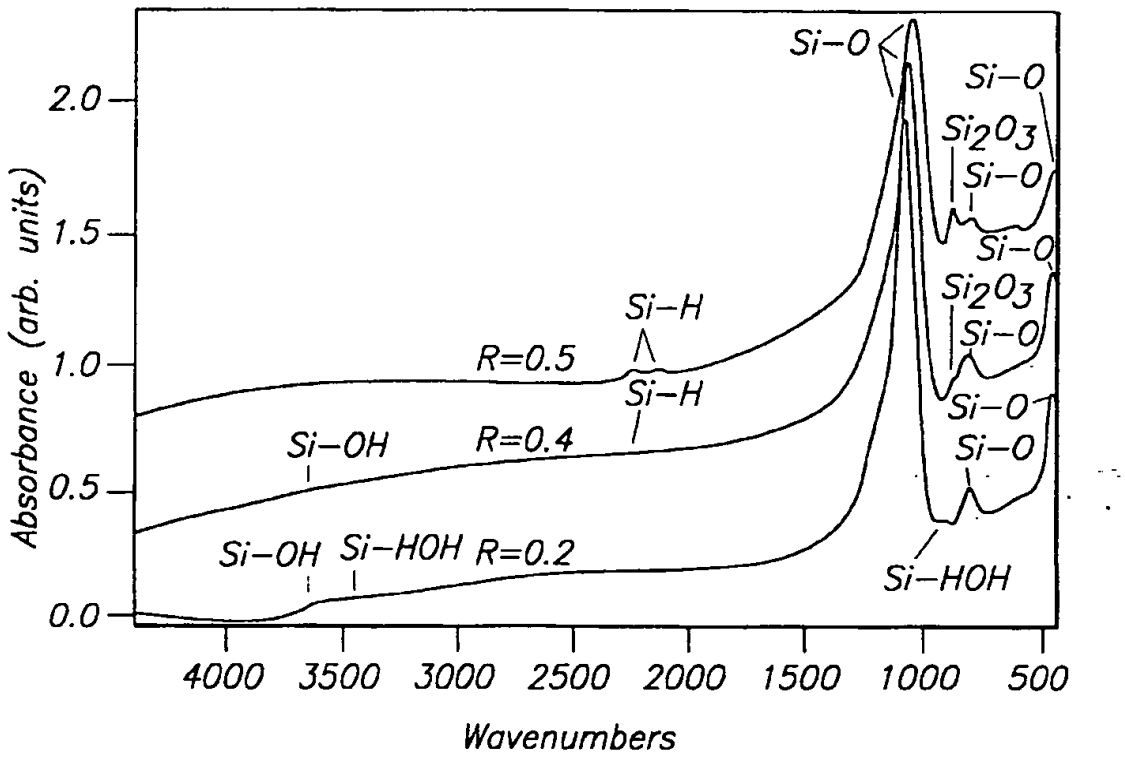
FIG. 1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0.0
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Wavenumbers
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Si–O
Si2O3
Si–O
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Si2O3
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Si–O
Si–H
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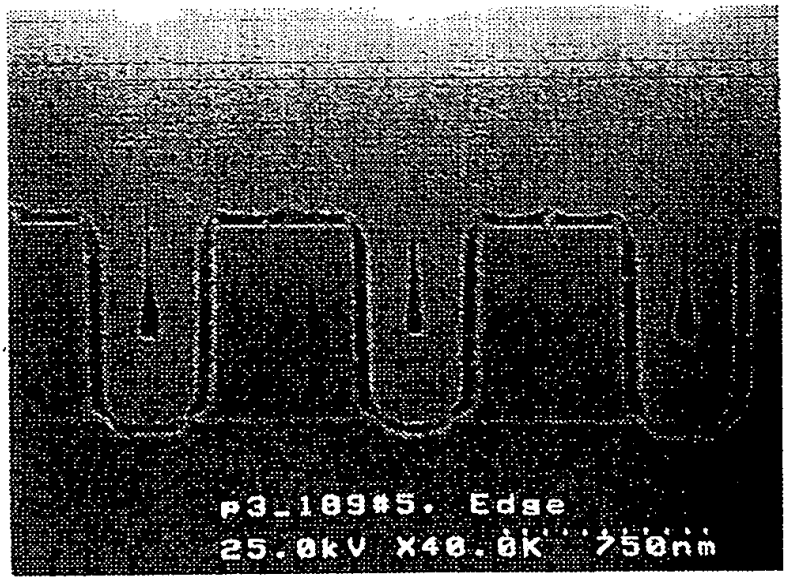
FIG. 2

FIG. 3A



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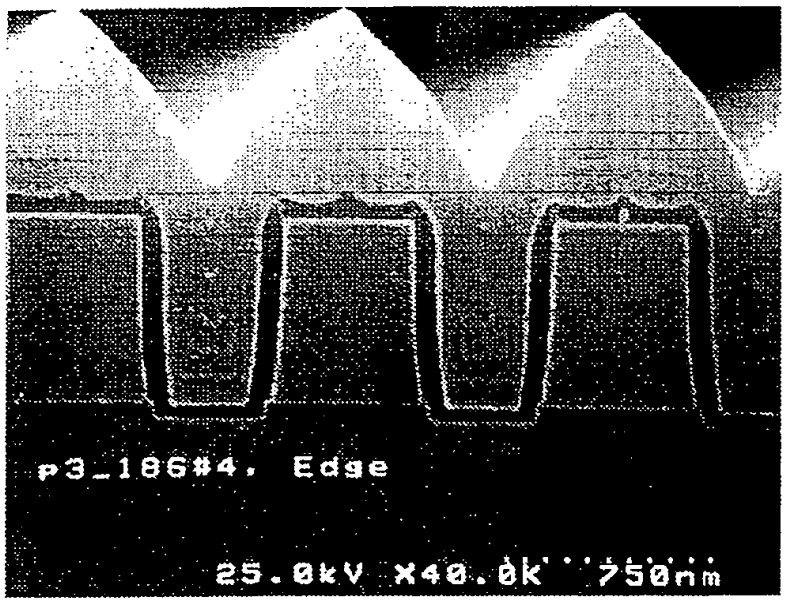
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FIG. 3C

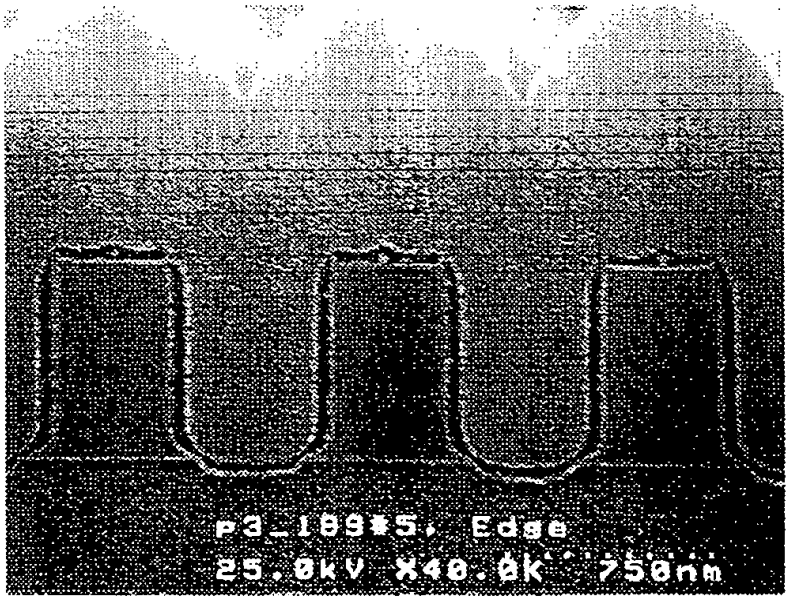
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FIG. 3D

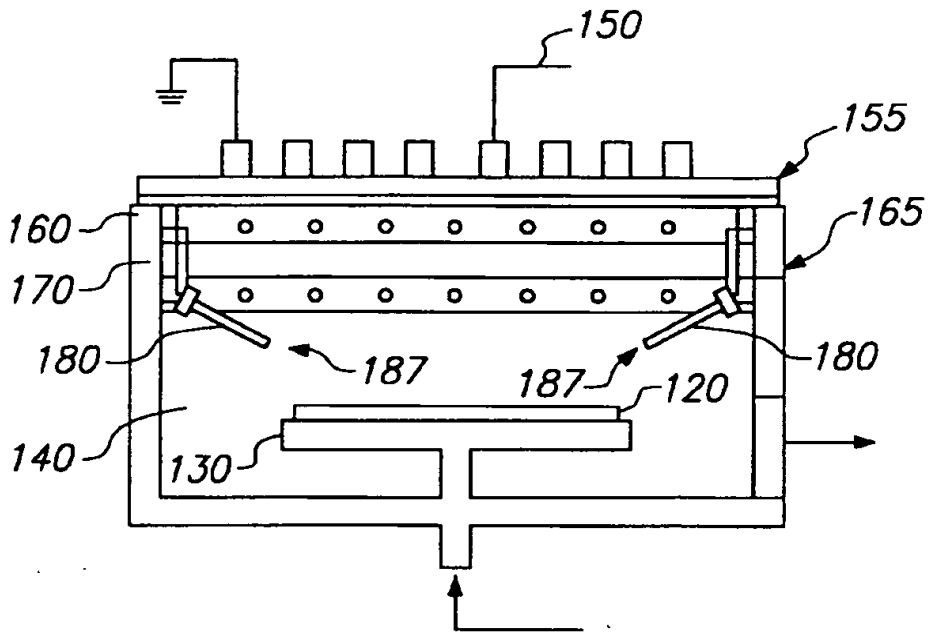
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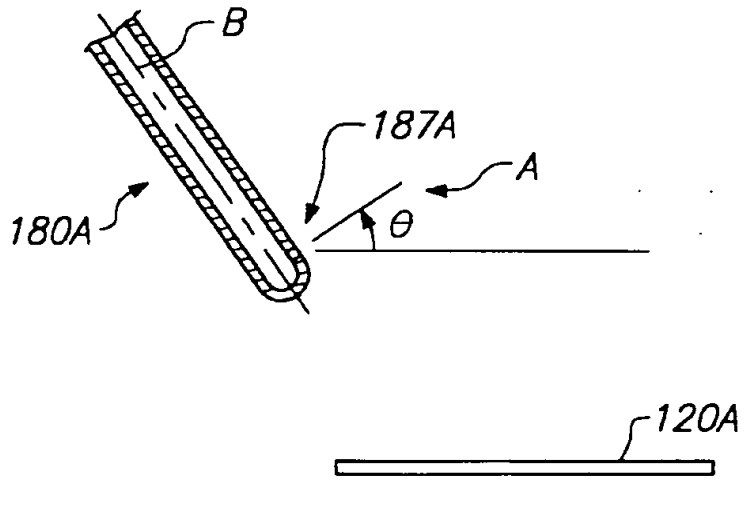
FIG. 4

FIG. 5


B
187A
A
θ
180A
120A

INDUCTIVELY COUPLED PLASMA CVD

FIELD OF THE INVENTION

The present invention relates to a method and apparatus for high-density plasma-enhanced chemical vapor deposition of semiconducting and dielectric films and more particularly to techniques for depositing such films into high aspect ratio gaps on semiconductor substrates such as silicon wafers having metal interconnection layers.

DESCRIPTION OF THE RELATED ART

Chemical vapor deposition (CVD) is conventionally used to form various thin films in a semiconductor integrated circuit. CVD can form thin films such as SiO_2, Si_3N_4, Si or the like with high purity and high quality. In the reaction process of forming a thin film, a reaction vessel in which semiconductor substrates are arranged can be heated to a high temperature condition of 500 to 1000° C. Raw material to be deposited can be supplied through the vessel in the form of gaseous constituents so that gaseous molecules are thermally dissociated and combined in the gas and on a surface of the substrates so as to form a thin film.

A plasma-enhanced CVD apparatus utilizes a plasma reaction to create a reaction similar to that of the above-described CVD apparatus, but at a relatively low temperature in order to form a thin film. The plasma CVD apparatus includes a process chamber consisting of a plasma generating chamber which may be separate from or part of a reaction chamber, a gas introduction system, and an exhaust system. Plasma is generated in such apparatus by various plasma sources. A substrate support is provided in the reaction chamber which may include a radio frequency (RF) biasing component to apply an RF bias to the substrate and a cooling mechanism in order to prevent a rise in temperature of the substrate due to the plasma action.

Vacuum processing chambers are generally used for chemical vapor depositing of materials on substrates by supplying deposition gas to the vacuum chamber and applying of an RF field to the gas. For example, parallel plate and electron-cyclotron resonance (ECR) reactors have been commercially employed. See U.S. Pat. Nos. 4,340,462 and 5,200,232. The substrates are held in place within the vacuum chamber during processing by substrate holders. Conventional substrate holders include mechanical clamps and electrostatic clamps (ESC). Examples of mechanical clamps and ESC substrate holders are provided in U.S. Pat. No. 5,262,029 and U.S. application Ser. No. 08/401,524 filed on Mar. 10, 1995.

Plasma-enhanced chemical vapor deposition (PECVD) has been used for depositing intermetal dielectric layers at low temperatures in integrated circuit applications. A publication by M. Gross et al. entitled "Silicon dioxide trench filling process in a radio-frequency hollow cathode reactor", J. Vac. Sci. Technol. B 11(2), March/April 1993, describes a process for void-free silicon dioxide filling of trenches using a hollow cathode reactor wherein silane gas is fed through a top target which supports a low frequency (1 MHz), low pressure (~0.2 Pa) oxygen and xenon discharge. In this process, high ion bombardment and a low rate of gas phase reaction produce an ion induced reaction with surface adsorbates, leading to directional oxide film growth whereby trenches with one micron openings and aspect ratios up to 2.5:1 are filled at rates over 400 Å/min.

A publication by P. Shufflebotham et al. entitled "Biased Electron Cyclotron Resonance Chemical-Vapor Deposition of Silicon Dioxide Inter-Metal Dielectric Thin Films," Materials Science Forum Vol. 140–142 (1993) describes a low-temperature single step gap-filled process for use in intermetal dielectric (IMD) applications on wafers up to 200 mm in diameter wherein sub –0.5 micron high aspect ratio gaps are filled with SiO_2 utilizing an O_2—Ar—SiH_4 gas mixture in a biased electron cyclotron resonance plasma-enhances chemical-vapor deposition (ECR-CVD) system. That single step process replaced sequential gap-filling and planarization steps wherein CVD SiO_2 was subjected to plasma etch-back steps, such technique being unsuitable for gap widths below 0.5 microns and aspect ratios (gap height:width) above 1.5:1.

Prior art apparatuses suffer from several serious disadvantages with respect to IMD applications. ECR and helicon sources which rely on magnetic fields are complex and expensive. Moreover, magnetic fields have been implicated to cause damage to semiconductor devices on the wafer. ECR, helicon and helical resonator sources also generate plasmas remotely from the wafer, making it very difficult to produce uniform and high quality films at the same time and also difficult to perform in-situ plasma cleans necessary to keep particulates under control without additional equipment. Furthermore, ECR, helicon and helical resonator, and domed inductively-coupled plasma systems require large, complex dielectric vacuum vessels. As a corollary scale-up is difficult and in-situ plasma cleaning is time consuming.

SUMMARY OF THE INVENTION

The present invention is directed to processes that employ an inductively coupled plasma-enhanced chemical vapor deposition (IC PECVD) high density plasma system. The system is compact, in-situ cleanable and produces high quality semiconductor and dielectric films.

In one aspect, the invention is directed to a method for filling gaps between electrically conductive lines on a semiconductor substrate comprising the steps of: providing a substrate in a process chamber of an inductively coupled plasma-enhanced chemical vapor deposition reactor which can include a substantially planar induction coil; introducing a process gas which can include a noble gas into the process chamber wherein the amount of noble gas is sufficient to assist in gap filling; and growing a dielectric film on the substrate with dielectric film being deposited in gaps between electrically conductive lines on the substrate.

In another aspect, the invention is directed to a method for filling gaps between electrically conductive lines on a semiconductor substrate comprising the steps of: providing a substrate in a process chamber of an inductively coupled plasma-enhanced chemical vapor deposition reactor which can include a substantially planar induction coil; filling gaps between electrically conductive lines on the substrate by: (i) introducing a first process gas which can include a noble gas into the process chamber wherein the amount of noble gas is sufficient to assist in gap filling; and (ii) growing a first dielectric film in the gaps at a first deposition rate; and depositing a capping layer comprising a second dielectric film onto the surface of said first dielectric film by introducing a second process gas into the process chamber, said capping layer being deposited at a second deposition rate that is higher than the first deposition rate.

In a further aspect, the invention is directed to a method of depositing a dielectric film on a substrate comprising the steps of: providing a substrate in a process chamber of an inductively coupled plasma-enhanced chemical vapor deposition reactor wherein the substrate is positioned on a substrate holder; introducing a process gas which can

include a noble gas into the process chamber, wherein the amount of noble gas is sufficient to assist in depositing the dielectric film; controlling the temperature on a surface of the substrate holder; and energizing the process gas into a plasma state by inductively coupling RF energy into the process chamber and growing a dielectric film on the substrate.

In yet another aspect, the invention is directed to an inductively coupled plasma processing system comprising: a plasma processing chamber, a substrate holder supporting a substrate within said processing chamber wherein the substrate holder is at a temperature of about 80° C. to 200° C., an electrically-conductive coil that is disposed outside said processing chamber; means for introducing a process gas into said processing chamber; and an RF energy source which inductively couples RF energy into the processing chamber to energize the process gas into a plasma state. Planar and non-planar coils can be employed however, a substantially planar coil is preferred.

Depending on the film to be deposited, the process gas may comprise a silicon-containing reactant gas selected from the group consisting of SiH_4, SiF_4, Si_2H_6, TEOS, TMCTS, and mixtures thereof. The process gas may comprise a reactant gas selected from the group consisting of H_2, O_2, N_2, NH_3, NF_3, N_2O, and NO, and mixtures thereof. Alternatively, the process gas may comprises a reactant gas selected from the group consisting of boron-containing gas, phosphorous-containing gas, and mixtures thereof. Most preferably, the process gas may also include a noble gas such as argon.

According to one feature of the invention, the inductively coupled plasma is generated by an RF antenna having a planar coil design. Thus, the IC PECVD reactor can be easily scaled up to accommodate, for example, 300 mm wafers and 600 mm×720 mm flat panel displays. The inductively coupled plasma (ICP) source generates uniform, high density plasmas over large areas independently of the bias power used to control the ion sputter energy. Unlike ECR or helicon sources, no magnets are required.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in greater detail with reference to the accompanying drawings in which like elements bear like reference numerals, and wherein:

FIG. 1 is a schematic of a high density inductively coupled plasma reactor which can be used to carry out the process according to the invention;

FIG. 2 comprises FTIR spectra of films deposited at various oxygen to silane mass flow ratios (constant total flow).

FIGS. 3A, 3B, 3C, and 3D are scanning electron microscopy (SEM) images of gap fills wherein all samples were decorated to enhance imperfections in the film; the structures were polysilicon on oxide and all depositions were for 3 minutes, except that of 3A, which was for 1 minute;

FIG. 4 illustrates a plasma reactor with a gas injection system; and

FIG. 5 illustrates an injector for the gas injection system.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Inductively Coupled Plasma-Enhanced CVD Reactor

FIG. 1 shows a ICP reactor **20** which can process substrates with high density plasma. Suitable ICP reactors include TCP™ systems from LAM Research Corp., Fremont, Calif. See also Ogle, U.S. Pat. No. 4,948,458 which is incorporated herein. The reactor includes a process chamber **21** in which plasma **22** is generated adjacent substrate **23**. The substrate is supported on water cooled substrate support **24** and temperature control of the substrate is achieved by supplying helium gas through conduit **25** to a space between the substrate and the substrate support. The substrate support can comprise an anodized aluminum electrode, which may be heated, or a ceramic material having a buried electrode therein, the electrode being powered by an RF source **26** and associated circuitry **27** for providing RF matching, etc. The temperature of the substrate during processing thereof is monitored by temperature monitoring equipment **28** attached to temperature probe **29**.

In order to provide a vacuum in chamber **21**, a turbo pump is connected to outlet port **30** and a pressure control valve can be used to maintain the desired vacuum pressure. Process gases can be supplied into the chamber by conduits **31, 32** which feed the reactant gases to gas distribution rings extending around the underside of dielectric window **33** or the process gases can be supplied through a dielectric showerhead window. An external ICP coil **34** located outside the chamber in the vicinity of the window is supplied with RF power by RF source **35** and associated circuitry **36** for impedance matching, etc. As is apparent, the external induction coil is substantially planar and generally comprises a single conductive element formed into a planar spiral or a series of concentric rings. The planar configuration allows the coil to be readily scaled-up by employing a longer conductive element to increase the coil diameter and therefore accommodate larger substrates or multiple coil arrangements could be used to generate a uniform plasma over a wide area. When a substrate is processed in the chamber, the RF source **35** supplies the coil **34** with RF current preferably at a range of about 100 kHz–27 MHz, and more preferably at 13.56 MHz and the RF source **26** supplies the lower electrode with RF current preferably at a range of about 100 kHz–27 MHz, and more preferably at 400 kHz, 4 MHz or 13.56 MHz. A large DC sheath voltage above the surface of a substrate can be provided by supplying RF power to the electrode.

RF bias is applied to the substrate to generate ion bombardment of the growing film during the gap filling step. The RF frequency can be anything above the value necessary to sustain a steady state sheath, which is a few hundred kHz. Substrate bias has numerous beneficial effects on film properties, and can also be used to simultaneously sputter the growing film in the gap-fill step. This allows narrow, high aspect ratio gaps to be rapidly filled with high quality dielectric. RF bias can be used during the cap layer deposition step.

Reactor **20** can be used to carry out the gap filling process of the invention wherein a heavy noble gas is used to increase the etch-to-deposition rate ratio (EDR) for void-free filling of sub 0.5 μm high aspect ratio gaps. Gap filling processes are further described in copending application Ser. No. 08/623,825 filed on Mar. 29, 1996 entitled "IMPROVED METHOD OF HIGH DENSITY PLASMA CVD GAP-FILLING," which application is incorporated herein. The heavy noble gas is effective in sputtering corners of sidewalls of the gaps such that the corners are facetted at an angle of about 45 degrees. The noble gas has a low ionization potential and forms massive ions which enhance the sputtering rate at a given RF power relative to the deposition rate, thus reducing the power required to fill a given gap structure. Moreover, the low ionization potential of the noble gas helps spread plasma generation and ion

bombardment more uniformly across the substrate. As xenon is the heaviest of the non-reactive noble gasses, xenon is preferred as the noble gas. Krypton can also be used even though it has a lower mass and higher ionization potential than xenon. Argon is also suitable as the noble gas. Preferably, the amount of noble gas added is effective to provide a sputter etch component with a magnitude on the order of the deposition rate such that the etch to deposition rate ratio is preferably about 5% to 70%, and more preferably about 10% to 40%.

In carrying out the deposition process in a ICP-CVD reactor, the chamber can be maintained at a vacuum pressure of less than 100 mTorr and preferably 30 mTorr or less and more preferably from about 1 mTorr to 5 mTorr. The flow rates of the individual components of the process gas typically ranges from 10 to 200 sccm for a 200 mm substrate and higher for larger substrates. A turbomolecular pump throttled by a gate valve is used to control the process pressure. The relative amount of each component will depend, in part, on the stoichiometry of the compound(s) to be deposited. The ICP power preferably ranges from 200 to 3000 watts, and the RF bias power applied to the bottom electrode can range from 0 to 3000 watts for a 200 mm substrate. Preferably the bottom electrode has a surface area so that the RF bias power can supply about 0–8 watts/cm^2 and preferably at least 2 watts/cm^2 of power. A heat transfer gas comprising, for example, helium and/or argon can be supplied at a pressure of 1 to 10 Torr to preferably maintain the substrate temperature at about −20° C. to 500° C., and more preferably at about 100° C. to 400° C. and most preferably about 150° C. to 375° C.

In order to prevent damage to metal lines or the pre-existing films and structures on the substrate and to ensure accurate and precise process control, a heated mechanical or preferably an electrostatic chuck (ESC) is employed to hold the substrate. The ESC is preferably bipolar or monopolar. Preferably, the electrode is maintained at a temperature ranging from about 50° C. to 350° C., in order to maintain the temperature of the wafer to about 325° C. to 375° C. The preferred electrode temperature will depend on, among other things, the RF bias level and the particular deposition step. For example, during the gap-fill process, the electrode temperature is preferably maintained between about 80° C. (full bias) to 200° C. (no bias). Similarly, during the capping process, the electrode temperature is preferably maintained at between about 125° C. (full bias) to 350° C. (no bias). The gap-fulling and capping processes are described herein. A suitable chuck for temperature control is disclosed in copending application Ser. No. 08/724,005, filed on Sep. 30, 1996, entitled "VARIABLE HIGH TEMPERATURE CHUCK FOR HIGH DENSITY PLASMA CHEMICAL VAPOR DEPOSITION", by Brian McMillin, which is incorporated herein, now U.S. Pat. No. 5,835,334.

During deposition the substrate (e.g., wafer) is typically maintained at a temperature that is higher than that of the ESC due to the plasma heating. Consequently, even though the ESC may be heated, its temperature is lower than that of the substrate. The electrode preferably also provides for helium backside cooling for substrate temperature control. The substrate temperature may be controlled by regulating the level of the RF bias and the ESC temperature and other parameters as described herein. As further described in the experiments herein, the electrode temperature can significantly influence the physical properties of the film deposited.

ICP-CVD reactor is particularly suited for depositing SiO_2 for IMD applications as the films produced are of excellent quality that are practically indistinguishable from SiO_2 grown by high temperature thermal oxidation of crystalline Si (thermal oxide). In addition, the technique can fill gaps as narrow as 0.25 μm at aspect ratios of 3:1 and higher with high quality material. Furthermore, deposition temperatures can be below 450° C. for compatibility with Al metallizations and thickness uniformities are better than 2% 1-σ on 8 in. (20.32 cm) wafers, with substantially no variations in other film properties. Finally, in terms of process manufacturability, ICP-CVD can achieve net deposition rates above 5,000 Å/min in the gap fill process. For the cap layer, ICP-CVD can provide a deposition rate up to about 1.51 km/min with good uniformity. It is understood that conductor lines can be made from other suitable materials, including, for example, copper, tungsten, and mixture thereof.

The deposition of SiO_2 into sub–0.5 micron high aspect ratio gaps by the inventive process involves the simultaneous deposition and sputtering of SiO_2. The resultant anisotropic deposition fills gaps from the bottom-up and the angular dependence of the sputtering yield also prevents the tops of the gaps from pinching off during deposition. An important feature of most high density plasma systems is that the bias power determines the sheath voltage above the wafer essentially independently of plasma generation. High bias powers generate large sheath voltages, and thus energetic ion bombardment of the wafer surface. In the absence of an RF bias, the film quality and gap-filling performance tend to be poor due to a jagged appearance of the sidewall film suggesting that it is very porous and heavy deposits forming above metal lines shadow the trench bottoms from deposition and eventually pinch-off the gap, leaving a void.

ICP can generate a high density plasma (e.g., >about 1×10^{11} ions/cm^3) and sustain it even at a very low pressure (e.g., <about 10 mTorr). The advantages of high density PECVD include increased throughput, uniform ion and radical densities over large areas, and subsequent manufacturability of scaled-up reactors. When complemented with a separate RF biasing of the substrate electrode, ICP-CVD systems also allow independent control of ion bombardment energy and provide an additional degree of freedom to manipulate the plasma deposition process.

In ICP systems, SiO_2 film growth occurs by an ion-activated reaction between oxygen species impinging onto the wafer from the plasma source and silane fragments adsorbed on the wafer. Using ICP-CVD, sub–0.5 μm, high aspect ratio gaps can be filled with high quality SiO_2 dielectric on 8 in. (20.32 cm) diameter wafers. In essence, the ICP-CVD system provides a manufacturable intermetal dielectric CVD process that utilizes high density plasmas.

Process Gas Distribution System

It has been demonstrated that for high density PECVD, improved deposition rate and uniformity can be achieved by employing a gas distribution system which provides uniform, high flow rate delivery of reactant gases onto the substrate surface, to both increase the deposition rate and to minimize the chamber cleaning requirements. A suitable gas distribution system is disclosed in copending application Ser. No. 08/672,315, filed on Jun. 28, 1996, entitled "FOCUSED AND THERMALLY CONTROLLED PLASMA PROCESSING SYSTEM AND METHOD FOR HIGH DENSITY PLASMA CHEMICAL VAPOR DEPOSITION OF DIELECTRIC FILMS," by Brian McMillin et al., which application is incorporated herein.

FIG. 4 illustrates a plasma processing system comprising such a gas distribution system. The system includes a substrate support 130 and processing chamber 140. The

support may comprise, for example, an RF biased electrode. The support may be supported from a lower endwall of the chamber or may be cantilevered, extending from a sidewall of the chamber. The substrate **120** may be clamped to the electrode either mechanically or electrostatically.

The system further includes an antenna **150**, such as the planar multiturn coil shown in FIG. **4**, a non-planar multiturn coil, or an antenna having another shape, powered by a suitable RF source and suitable RF impedance matching circuitry inductively couples RF energy into the chamber to provide a high density plasma. The chamber may include a suitable vacuum pumping apparatus for maintaining the interior of the chamber at a desired pressure. A dielectric window, such as the planar dielectric window **155** of uniform thickness shown in FIG. **4**, or a non-planar dielectric window, is provided between the antenna **150** and the interior of the processing chamber **140** and forms the vacuum wall at the top of the processing chamber.

A primary gas ring **170** is provided below the dielectric window **155**. The gas ring **170** may be mechanically attached to the chamber housing above the substrate. The gas ring **170** may be made of, for example, aluminum or anodized aluminum.

A secondary gas ring **160** may also be provided below the dielectric window **155**. One or more gases such as Ar and O_2 are delivered into the chamber **140** through outlets in the secondary gas ring **160**. Any suitable gas ring may be used as the secondary gas ring **160**. The secondary gas ring **160** may be located above the gas ring **170**, separated by an optional spacer **165** formed of aluminum or anodized aluminum, as shown in FIG. **4**.

Alternatively, although not shown, the secondary gas ring **160** may be located below the gas ring **170**, in between the gas ring **170** and the substrate **120**, or the secondary gas ring **160** may be located below the substrate **120** and oriented to inject gas vertically from the chamber floor. Yet another alternative is that the Ar and O_2 may be supplied through outlets connected to the chamber floor, with the spacer **165** separating the dielectric window **155** and the primary gas ring **170**.

A plurality of detachable injectors **180** are connected to the primary gas ring **170** to direct a process gas such as SiH_4 or a related silicon-containing gas such as SiF_4, TEOS, and so on, onto the substrate **120**. These gases are delivered to the substrate from the injectors **180** through injector exit orifices **187**. Additionally, reactant gases may be delivered through outlets in the primary gas ring **170**. The injectors may be made of any suitable material such as aluminum, anodized aluminum, quartz or ceramics such as Al_2O_3. Although two injectors are shown, any number of injectors may be used. For example, an injector may be connected to each of the outlets on the primary gas ring **170**. Preferably, eight to thirty-two injectors are employed on a 200 to 210 mm diameter ring **170** for a 200 mm substrate.

The injectors **180** are located above the plane of the substrate **120**, with their orifices at any suitable distance such as, for example, 3 to 10 cm from the substrate. The injectors may, according to a preferred embodiment, be spaced inside or outside of the substrate periphery, for example, 0 to 5 cm from the substrate periphery. This helps to ensure that any potential particle flakes from the injectors will not fall onto the substrate and contaminate it. The injectors may all be the same length or alternatively a combination of different lengths can be used to enhance the deposition rate and uniformity. The injectors are preferably oriented such that at least some of the injectors direct the process gas in a direction which intersects the exposed surface of the substrate.

As opposed to previous gas injection systems designs which rely predominantly on diffusion to distribute gas above the substrate, the injectors according to one embodiment of the present invention are oriented to inject gas in a direction which intersects an exposed surface of the substrate at an acute angle. The angle of injection may range from about 15 to <90 degrees, preferably 15 to 45 degrees from the horizontal plane of the substrate. The angle or axis of injection may be along the axis of the injector or, alternatively, at an angle of up to 90 degrees or more with respect to the axis of the injector. The exit orifice diameter of the injectors may be between 0.010 and 0.060 inches, preferably about 0.020 to 0.040 inches. The hollow core of the injectors **180** may be drilled to about twice the diameter of the exit orifices **187** to ensure that sonic flow occurs at the exit orifice and not within the core of the injector. The flow rate of SiH_4 is preferably between 25–300 sccm for a 200 mm substrate but could be higher for larger substrates.

Another gas injection system that can be used employs a plurality of injectors as illustrated in FIG. **5**. In this embodiment, the orifice **187A** is oriented to introduce the gas along an axis of injection (designated "A") in a direction pointing away from the wafer **120A** (and toward the dielectric window). The angle or axis of injection may be along the axis of the injector (designated "B") or, alternatively, at an angle of up to about 90 degrees or higher with respect to the axis of the injector. In this configuration, the axis of injection may range from about 5 to <90 degrees, preferably about 15 to 75 degrees, and most preferably, about 15 to 45 degrees from the plane of the substrate. This design retains the feature that the process gas is focused above the wafer which leads to high deposition rates and good uniformity, and further provides the advantage of reduced susceptibility to orifice clogging. The reduced potential of the orifice clogging thus allows more wafers to be processed before injector cleaning is required, which ultimately improves the wafer processing throughput.

Due to the small orifice size and number of injectors and large flowrates of SiH_4, a large pressure differential develops between the gas ring **170** and the chamber interior. For example, with the gas ring at a pressure of >1 Torr, and the chamber interior at a pressure of about 10 mTorr, the pressure differential is about 100:1. This results in choked, sonic flow at the outlets of the injectors. The interior orifice of the injector may also be contoured to provide supersonic flow at the outlet.

Injecting the SiH_4 at sonic velocity inhibits the plasma from penetrating the injectors. This design prevents plasma-induced decomposition of the SiH_4 and the subsequent formation of amorphous silicon residues within the gas ring and injector extension tubes.

EXPERIMENTAL

For gap filling and depositing a cap layer, the process generally comprises an initial optional sputter clean/pre-heat step in a plasma without any silicon-containing gas which is followed by a high bias power gap-fill step. After the gap has been partially filled, a final sacrificial or "cap" layer of film is deposited preferably at low RF bias power. Preferably, the gap-fill step fills substantially all or at least a major portion of the gap before the cap layer is deposited. The cap layer deposition step only requires enough bias power to keep the film quality adequate as no sputtering during film growth is required. The cap layer is deposited at a higher deposition rate than that of the gap-fill step. Preferably, this cap film is partially removed in a subsequent chemical-mechanical polishing (CMP) planarization step.

The IC PECVD system generates a high density, low pressure plasma in a process gas comprising components that form the semiconducting or dielectric, and cap films. The inventive process is applicable to depositing any suitable semiconducting, dielectric and/or cap film including, for example, hydrogenated amorphous silicon Si:H, silicon oxide SiO_x, where x is 1.5 to 2.5, silicon nitride, SiN, silicon oxyfluoride, SiO_xF_y where x is 1.5 to 2.5 and y is 2 to 12, and mixtures thereof. It is understood that both stoichiometric and non-stoichiometric compounds can be deposited and the values of x and y can be controlled by regulating the process parameters such as, for example, the choice of reactant gases and their relative flow rates. It is expected that inorganic and organic polymers can also be deposited. A preferred dielectric and cap film comprises SiO_2. While the invention will be illustrated by describing the deposition of SiO_2, it is understood that the invention is applicable to other films.

The components of the process gas will depend on the semiconducting and/or dielectric film to be deposited. With respect to silicon-containing films the process gas can comprise, for example, silane (SiH_4), tetraethylorthosilicate (TEOS), 1,3,5,7-tetramethylcyclotetrasiloxane (TMCTS), disilane (Si_2H_6) or other silicon-containing organometallic gases. The process gas may include a noble gas preferably Ar, Kr, Xe, and mixtures thereof to control plasma properties or sputtering rates particularly during the gap filling step prior to depositing the cap layer. To incorporate non-silicon components into the film, the process gas may include a reactant gas such as, for example, H_2, O_2, N_2, NH_3, NF_3, N_2O, NO and mixtures thereof. Reactant gases may also comprise boron and/or phosphorous containing gases to produce boro-phospho-silicate glass (BPSG), boro-silicate glass (BSG), and phospho-silicate gas (PSG) films.

EXAMPLE I

(Gap-filling process)

SiO_2 IMD depositions were conducted in an ICP system similar to that of FIG. 1. Mechanically-clamped 150 mm wafers were employed. Two gas rings located at the bottom edge of window **33** were employed. One ring distributed the SiH_4 and the other distributed the Ar and O_2. System parameters are set forth in Table 1. The electrode temperature was maintained at 80° C.

TABLE 1

ICP RF power:	1000 watts at 13.56 MHz
Electrode bias RF power	1900 watts at 400 kHz
Ar mass flow rate	100 sccm
O_2 mass flow rate	60 sccm
SiH_4 mass flow rate	40 sccm
Wafer backside He pressure	3 Torr
Chamber pressure	3.75 milli-Torr (1000 l/s pump)

Effect of Oxygen to Silane Mass Flow Ratio (at constant total flow) on Film Properties

The film stoichiometry was determined by the chemical composition of the plasma, established primarily by the ratio R of the silane and oxygen mass flow rates: $R=Q_{SiH4}/(Q_{SiH4}+Q_{O2})$ where Q is the gas mass flow rate. Note that the effective oxygen-silane ratio that the wafer sees also depended on other process parameters. The effect of R on the film properties is shown in Table 2.

TABLE 2

O_2 Flow Rate	SiH_4 Flow Rate	Ratio	Time	Dep. Rate	Stress	Film Refractive Index*			OH Content
sccm	sccm	%	sec	Å/min.	MPa	center	mid-radius	edge	at. %
60	40	0.40	180	3460	-91	1.4630	1.4628	1.4633	2.72
70	30	0.30	280	2585	-74	1.4574	1.4579	1.4579	9.10
55	45	0.45	132	3969	-115	1.5414	1.5376	1.5628	0.43
80	20	0.20							9.43
50	50	0.50	120	5449	-65				0.31
50	50	0.50	104	5527	-65	1.6269	1.6203		0.28
65	35	0.35	101	3284	-90				8.79
70	30	0.30	280	2613	-65	1.4574	1.4572	1.4572	9.45
60	40	0.40	180	3591	-106	1.4628	1.4635	1.4647	2.20
80	20	0.20	480	1513	-53	1.4572	1.4571	1.4572	9.08
65	35	0.35	223	3317	-87	1.4584	1.4578	1.4586	8.85
100	0	0.00	300	0					

*The refractive index was measured at the center, mid-radius and edge of each wafer.

The plasma chemistry for the deposition can be broadly classified into the following reactions:

$$R<0.5:\ SiH_4\text{-limited}\ (2+n)O_2+SiH_4\rightarrow SiO_2{:}(OH)_{4n}+(2-2n)H_2O \quad (I)$$

$$R\geq 0.5:\ O_2\text{-limited}\ O_2+SiH_4\rightarrow SiO_2{:}(H)_{2n}+(2-n)H_2 \quad (II)$$

Here, $SiO_2{:}(X)_n$ indicates an approximately stoichiometric oxide containing some fraction n of X, where $0\leqq n<1$. Based on the OH contents measured, n was always less than 0.025 (OH <10 at. %). Reaction (I) dominated as long as film growth was silane-limited ($R\leqq 0.5$). This reaction released increasing amounts of water into the plasma as R decreased, which accounts for the observation that the OH concentration in the films increased with decreasing R. Conversely, operating in the oxygen-limited regime, reaction (II) (R>0.5) resulted in increased H_2 production, which accounts for the increasing incorporation of H as Si—H (and the resulting appearance of Si-rich, sub-oxide groups such as Si_2O_3) at larger R. This also accounts for the higher chamber pressures measured at high R, since turbomolecular pumps have low pumping speeds in H_2.

The data also suggest that a significant change in the process takes place near R=0.40. This transition was evident in all film properties, as shown in Table 2, and appears to correspond to the transition from a silane-limited chemistry, reaction (I), to an oxygen-limited chemistry, reaction (II), discussed above. The deposition rate depended linearly on silane flow, and the silane-limited region (R<0.40) extrapolated to zero thickness at zero flow, as would be expected.

Film stress is typically a function of the mechanical stress due to differential thermal expansion between the film and substrate, and the intrinsic film stress. The former is primarily determined by the deposition temperature. In the latter case, the film micro-structure and stoichiometry were the dominant factors. In the SiH_4-limited regime, the film stress appeared to depend primarily on the deposition rate. It is believed that faster film growth allowed less time thermal relaxation and sputtering/densification by ion bombardment. Films grown under O_2-limited conditions were less compressive, even though deposited at higher deposition rates, than films grown under O_2-rich conditions.

The FTIR spectra, shown in FIG. 2, illustrate the relevance of reactions I and II. At low R, Si—OH and Si—HOH absorbance bands were observed, but not for Si—H. At high R, there was no detectable Si—OH, but both Si—H and sub-oxide (Si_2O_3) Si—O bands were present. At intermediate R, just on the O_2-rich side of the critical range, there appears to be minimal Si—OH and Si—H incorporation. The intermediate R range is optimum for achieving the desired dielectric constant. The refractive index can also be used as a gauge for the preferred operating conditions since refractive indices between 1.465 and 1.480 correspond to films having good dielectric constants.

Effect of ICP Power On Film Properties:

Table 3 shows how the film properties depend on the ICP power with the bias power held constant at 1000 W.

TABLE 3

ICP Power	Dep. Rate	Stress	SiO_x Refractive Index			OH Content
W	Å/min.	MPa	center	mid-radius	edge	at. %
1200	3295	−196	1.4659	1.4654	1.4659	3.81
800	3103	−138	1.4731	1.4738	1.4743	0.65
600	3117	−128	1.4731	1.4879	1.4866	0.43
400	3008	−139	1.5178	1.5151	1.5139	0.53
200	2731	−123	1.5610	1.5606	1.5675	0.51
1200	3396	−208	1.4693	1.4591	1.4640	3.95
200	2674	−113	1.5510	1.5507	1.5515	0.60
600	3060	−142	1.4796	1.4772	1.4746	0.55

The effect that ICP power has on film properties is similar in nature to that caused by the total flow. Both effects appear to essentially be a deposition precursor supply phenomenon. Assuming that the primary deposition precursor was generated through silane dissociation, the supply of this species on the wafer surface will depend on its rate of generation in the plasma and its rate of loss to the pump and to deposition on the reactor walls. Both the total flow and the ICP power could influence the effective R at the wafer through either generation or loss based mechanisms.

In the case of precursor generation, calculations based on bond strengths show that the energy required to dissociate SiH_4 should be less than that for O_2. In this case, increasing the silane supply (total flow) would preferentially increase the supply of SiH_x over any relevant oxygen species. This drives the reaction chemistry to higher R, as observed. The ICP power should also drive this process, although it is unclear what the dependence should be.

Effect of Bias Power on Film Properties

The bias power was applied to the wafer in order to increase the DC sheath potential, and thus the kinetic energy of the bombarding ions, to the point where they sputter the film as it grows. This improved the quality of the films in a variety of ways. O_2 plasma preceding deposition sputter cleans the wafer surface, allowing a clean, adherent interface to form. Since ion bombardment heats the wafer during deposition, temperature control requires He backside cooling. Ion bombardment also tends to preferentially sputter "etch" weak and nonequilibrium structures from the film, and to produce densification through compaction. This allows high quality films to be deposited at lower wafer temperatures than otherwise possible. The dependence of the film properties on bias power is shown in Table 4.

TABLE 4

RF Bias Power	Dep. Rate	Stress	Refractive Index			OH Content
Watts	Å/min.	MPa	center	mid-radius	edge	at. %
1	3850	−295	1.4756	1.4751	1.4763	2.28
1	3853	−301	1.4750	1.4749	1.4758	2.30
1	3842	−315	1.4756			2.56
100	3858	−334		1.4759		2.64
100	3883	−368		1.4761		2.57
100	3893	−361	1.4767			4.05
200	3823	−348		1.4763		3.38
400	3835	−317		1.4744		4.73
500	3722	−117	1.4653			4.90
600	3652	−104		1.4644		3.77
800	3613	−93		1.4639		2.88
1000	3345	−96	1.4633	1.4627	1.4639	2.40
1000	3505	−108	1.4628	1.4622	1.4635	2.31
1000	3350	−96	1.4623			2.69
1000	3538	−105	1.4633			2.25
1200	3393	−107	1.4636			2.06
1400	3336	−123	1.4645			1.34
1500	3159	−101	1.4633			1.79

It was observed that general film properties underwent a significant change between 400 and 500 watts. It is believed that although the ion energy may have increased with bias power below 400 W, the ions did not have sufficient energy to sputter, so the dominant effect of bias power in this regime was to enhance plasma generation above the wafer. Above 400 W, the average ion energy was presumably above the sputtering threshold for SiO_2, and the net deposition rate decreased as the sputtering component dominated any effects due to secondary plasma generation.

Gap-Fill Deposition

Gap-fill performance can be predicted from the "etch to deposition rate ratio", ER/DR, which is calculated from the deposition rates with and without RF bias (the "zero-bias" condition actually used 100 W to account for secondary plasma generation): E/D=[DR(no bias)−DR(bias)]+DR(no bias), (where DR denotes the deposition rate. Processes with higher E/D can fill more aggressive gaps. Generally, the lowest possible E/D that will fill the required gaps should be used in order to maximize the net deposition rate. Of course, once the gaps are filled, the E/D should be reduced to the minimum value needed to preserve film quality, thus allowing the majority of the IMD layer to be deposited at much higher rates.

The SEMs shown in FIGS. 3A, 3B, 3C, and 3D show examples of good and bad gap-fill by ICP-CVD. FIG. 3A shows a partial fill attempted with no bias power. The porous film morphology and the "breadloaf" appearance of the film can be seen at the top of the line. This eventually closes over to leave a void like that shown in FIG. 3B. These are also the structures that are preferentially sputtered away, since the sputtering yield is a maximum at 45°. FIG. 3B gives an example of unsuccessful fill where bias power was used, but the E/D was too low for the gap. Note that the breadloaves closed early in the process, leaving a large, deep gap. In FIG. 3C a tiny void formed just before the gap filled can be seen next to an otherwise identical gap that filled successfully. In

this case E/D was marginal. The layering was done deliberately by depositing a thin Si-rich layer periodically and decorating the sample with the appropriate stain to bring out the composition contrast. This clearly shows how the gap fills from the bottom up, with little sidewall growth compared to that on horizontal surfaces. The 45° facets formed above the lines by sputtering are also clearly visible. FIG. 3D shows how a moderate E/D process (100 sccm Ar) completely filled an aggressive gap. This shows that ICP-CVD can fill aggressive structures.

EXAMPLE II

(GaM-fill and Capping Processes)

SiO_2 IMD and capping depositions were conducted in an ICP system similar to that of FIG. 4. In this example 200 mm wafers were processed. The wafers were electrostatically clamped to a thermally controlled chuck. The lower electrode was powered by a 13.56 MHz generator. A 2000 l/sec pump to improve the pumping speed at high flows was also implemented into the ICP/CVD system. ICP power ranging from 1000 to 2500 watts was used. High bias power was used for the gap fill process and ranged from 500 to 2500 watts.

Typical process parameters are shown in Table 5 for the gapfill, cap, and sacrificial cap layers and the corresponding film characteristics. The table also lists the preferred ranges for the process parameters.

In the prior art, increasing the source and bias power have been used to increase the substrate temperature in an attempt to improve film quality. However, this often leads to a tradeoff amoung the desired film properties as demonstrated by the results below which examine the effect of helium backside pressure, power and chamber height.

Effect of Helium Backside Pressure Power and Chamber Height

A series of depositions were conducted wherein spacer height, helium cooling pressure and power level of the ICP-CVD device were varied to modulate the substrate temperature with an 80° C. electrode temperature. Table 6 presents the results. Substrate temperatures near 400° C. were found to produce high quality oxides. Among other things, a high substrate temperature drives off volatile species and improves film density. For deposition 3 where no helium was used, it was estimated that the wafer temperature was over 450° C.

In the first three-wafer set, the helium pressure was reduced from 2 Torr to 0 Torr (i.e. no cooling) and this caused an increase in the substrate temperature range from 275° C. to over 400° C. The film characteristics indicated that high wafer temperatures produced high quality film. Low OH levels were found in the films and all of the other film properties were excellent. The advantage of using high wafer temperature is that it does not cause adverse effects with respect to the film stress, OH % and wet etch ratio.

TABLE 5

	Gap-Fill	Cap-layer	Sacrificial Cap-Layer
Process Parameter			
Pressure (mT)*	5 (1–5)	14 (5–30)	12 (5–30)
ICP Power (watts)	2500 (1000–3500)	2500 (1000–3500)	2500 (1000–3500)
Bias Power (watts)	2000 (1000–3000)	2000 (1000–3000)	0 (0–3000)
Ar (sccm)	50 (0–100)	0 (0–100)	100 (0–200)
O_2 (sccm)	80 (25–150)	350 (150–500)	300 (150–300)
SiH_4 (sccm)	60 (20–200)	250 (80–400)	200 (80–400)
Electrode temp. (° C.)	120 (60–200)	120 (60–200)	120 (60–200)
Backside He Pressure (Torr)	1 (~0–6)	1 (~0–6)	1 (~0–6)
*Preferred ranges are provided in (parenthesis)			
Film Characteristics			
Deposition Rate (Å/min)	8080	11300	10700
Uniformity (% 1 sigma)	3.7%	3.8%	2.5%
Film Index	1.47	1.47	1.47
Uniformity of Index (% 1 sigma)	<1%	<1%	<1%
Stress (MPa)	-170	-172	-111
% OH	<2%	<1%	<1%
Wet Etch Rate SiO_2 = 1.0	<2:1	<2:1	3.5:1

In these depositions (0.5 μm gaps), argon was included in the process gas. However, the addition of argon is not always necessary as indicated in the preferred ranges. In the deposition of the cap layer, the initial deposition can employ a high electrode RF bias power to produce a good quality film. Thereafter, a lower bias power can be applied (preferably while maintaining about the same electrode temperature) to produce a sacrificial cap layer of lesser quality. Typically this sacrificial cap layer is substantially removed in a subsequent planarization process.

Generally a higher substrate temperature improves deposited film properties. Typically, there are two primary contributors to the substrate temperature: (1) thermal heating from the substrate support (ESC) and (2) plasma heating which comes primarily from the electrode RF bias power and, to a lesser extent, from the source (ICP, ECR, etc) power.

The second set of wafers (deposition no. 4, 5 and 6) demonstrate the effects of using helium and argon cooling gas for substrate temperature control. The first 3-wafer set used helium, and the second set of three wafers used argon for cooling. The results show that helium and argon produced similar process results.

The first and third set of 3-wafers compare the effect of plasma heating of the wafer. The wafer heating was accomplished by decreasing the distance between the ICP coil to the substrate surface (spacer height). The results indicated that film quality changed going from high to lower gap spacing for the same power level process. The OH% remained the same and the wet etch ratio improved at lower spacing comparing the 2 or 1 Torr helium cooling case. However, more compressive stress was observed when lower gap spacing was used.

When comparing the third 3-wafer set to the last 2 wafers in Table 6, the ICP power was decreased from 2500 to 2000

watts. The data show that less compressive stress was observed by decreasing the power. The wet etch ratio was degraded indicating that less plasma heating changed the film structure possibly making the film more porous. Therefore, the wet etch ratio is better at higher power levels.

TABLE 6

	Process conditions	Dep. rate Å/min	Uniformity (% 1-Sigma)	Film Ref. Index	Stress (MPa)	OH content (at %)	Wet etch ratio
1	6/2/2500	9371	3.63%	1.477	-246	1.7%	7.38
2	6/1/2500	9317	3.60%	1.480	-195	1.3%	6.67
3	6/0/2500	8129	2.83%	1.482	-65	0.3%	1.83
4	6/2/2500	9419	3.68%	1.478	-242	0.46%	8.02
5	6/1/2500	9420	3.65%	1.475	-175	0.88%	7.64
6	6/1/2500	9452	3.53%	1.472	-219	1.37%	7.98
7	0/2/2500	9146	6.47%	1.479	-377	1.0%	3.67
8	0/1/2500	9111	6.35%	1.478	-349	2.5%	3.22
9	0/3/2500	9159	6.60%	1.477	-370	0.4%	3.40
10	0/2/2000	8884	4.53%	1.479	-227	1.1%	5.29
11	0/1/2000	8870	4.86%	1.478	-168	0.1%	4.97

*The process conditions were spacer height (cm), helium cooling pressure (Torr), and (3) ICP power (watts). The RF bias was zero for each case.

Effect of Heated Electrode on Film Properties

In contrast to the approach of using the source and bias powers to increase the substrate temperature, it was demonstrated that using a higher electrode temperature can lead to improved film quality and a wider process window, without a tradeoff among the desired values of film stress, OH% and/or wet etch ratio.

This is illustrated by the results shown in Table 7, where cap layer deposition results with a 70 and 120° C. electrode are summarized for cases with and without an applied RF bias. Preferably, in preparing a cap layer film the wet etch ratio is <2:1, the OH% is ≦about 1%, and the magnitude of film stress is less than 200 Mpa. Simply increasing the plasma heating of the wafer by increasing the bias from 0 to 2000 W leads to a decrease in the wet etch ratio, but this also leads to an undesirable increase in film stress. In contrast, by using a higher temperature electrode, both the film stress and wet etch ratio are reduced for cases with and without RF bias power. Hence, a preferred process uses a thermally controlled electrode with a temperature that is selectable from the range of about 60 to 200° C.

TABLE 7

Comparison of film properties with 70 and 120° C. electrodes

	Wafer Temp (° C.)		Stress (MPa)		% OH		Wet Etch Rate Ratio	
	70° ESC	120° ESC	70° ESC	120° ESC	70° ESC	120° ESC	70° ESC	120° ESC
Cap Layer with bias	340	375	-250	-190	1.8	0.7	1.5	1.3
Cap Layer w/out bias	140	170	-193	-128	1.9	1.4	3.8	2.7

Process parameters used are set forth is Table 5

Another benefit of employing a higher electrode temperature is that the ranges for the other process conditions including, for example, pressure, reactant gas flow rates, and TCP power are wider so that a broader set of operating conditions can be employed.

The foregoing has described the principles, preferred embodiments and modes of operation of the present invention. However, the invention should not be construed as being limited to the particular embodiments discussed. Thus, the above-described embodiments should be regarded as illustrative rather than restrictive, and it should be appreciated that variations may be made in those embodiments by workers skilled in the art without departing from the scope of the present invention as defined by the following claims.

What is claimed is:

1. A method of filling gaps between electrically conductive lines on a semiconductor substrate comprising the steps of:

providing a substrate in a process chamber of an inductively coupled plasma-enhanced chemical vapor deposition (PECVD) reactor that comprises a substantially planar induction coil that generates a plasma;

introducing a process gas comprising a noble gas into the process chamber wherein the amount of noble gas is sufficient to assist in gap filling;

applying a radio frequency bias to the substrate; and

growing a dielectric film by PECVD on the substrate, wherein the dielectric film fills substantially the gaps between electrically conductive lines on the substrate and wherein the gaps have a diameter of less than 0.5 μm.

2. The method of claim 1, wherein the process gas further comprises a silicon-containing reactant gas selected from the group consisting of SiH_4, SiF_4, Si_2H_6, TEOS, TMCTS, and mixtures thereof, said process further comprising decomposing the silicon-containing reactant to form a silicon containing gas and plasma phase reacting said silicon-containing gas on a surface of the substrate.

3. The method of claim 2, wherein the process gas comprises a reactant gas selected from the group consisting of H_2, O_2, N_2, NH_3, NF_3, N_2O, and NO, and mixtures thereof.

4. The method of claim 2, wherein the process gas comprises a reactant gas selected from the group consisting of boron-containing gas, phosphorous-containing gas, and mixtures thereof.

5. The method of claim 3, wherein the process gas comprises a reactant gas selected from the group consisting of boron-containing gas, phosphorous-containing gas, and mixtures thereof.

6. The method of claim 1, wherein the vacuum is maintained at about 1 mTorr to about 30 mTorr.

7. The method of claim 1, wherein the film is deposited on a silicon wafer and the gaps are between conductor lines comprising aluminum, copper, tungsten, and mixtures thereof.

8. The method of claim 1, wherein the step of applying a radio frequency bias to the substrate comprises supporting the substrate on a substrate holder having an electrode supplying a radio frequency bias to the substrate, the radio frequency bias being generated by supplying the electrode with at least 2 watts/cm^2 of power.

9. The method of claim 1, wherein the radio frequency bias applied to the a substrate is at a frequency of between about 100 kHz to 27 MHz.

10. The method of claim 1, wherein the substrate is positioned on a substrate holder that is maintained at a temperature of about 80° C. to 200° C.

11. The method of claim 1, further comprising supplying a heat transfer gas between a surface of the substrate and a surface of a substrate support on which the substrate is supported during the film growing step.

12. The method of claim 11, further comprising clamping the substrate on an electrostatic or mechanical chuck during the film growing step.

13. The method of claim 12, wherein heat transfer gas which comprises helium and/or argon is supplied to a space between a surface of the substrate and a surface of the chuck.

14. The method of claim 1, further comprising plasma phase reacting an oxygen-containing gas in the gaps and removing polymer residues in the gaps prior to the film growing step.

15. The method of claim 1, wherein the dielectric film comprises silicon oxide.

16. The method of claim 1 wherein the dielectric film comprises SiO_2.

17. The method of claim 1, wherein the process gas includes a silicon and fluorine-containing reactants and the dielectric film comprises silicon oxyfluoride.

18. The method of claim 1, wherein the gas mixture includes a nitrogen-containing gas and the dielectric film comprises silicon oxynitride.

19. The method of claim 1, wherein the process gas is introduced through a gas supply including orifices, at least some of the orifices orienting the process gas along an axis of injection which intersects an exposed surface of the substrate at an acute angle.

20. The method of claim 19, wherein the step of introducing a process gas comprises the step of supplying a gas or gas mixture from a primary gas ring, wherein at least some of said gas or gas mixture is directed toward said substrate.

21. The method of claim 20, wherein the step of introducing the gas further comprises the step of supplying an additional gas or gas mixture from a secondary gas ring.

22. The method of claim 20, wherein injectors are connected to said primary gas ring, the injectors injecting at least some of said gas or gas mixture into said chamber and directed toward the substrate.

23. A method of filling gaps between electrically conductive lines on a semiconductor substrate and depositing a capping layer over the filled gaps comprising the steps of:

providing a substrate in a process chamber of an inductively coupled plasma-enhanced chemical vapor deposition (PECVD) reactor that comprises a substantially planar induction coil that generates a plasma;

filling gaps between electrically conductive lines on the substrate by PECVD by introducing a first process gas comprising a noble gas and growing a first dielectric film in the gaps at a first deposition rate; and

after filling a major portion or substantially all of the each gap with the first dielectric film, depositing by PECVD a capping layer comprising a second dielectric film onto the surface of said first dielectric film by introducing a second process gas comprising a noble gas into the process chamber, said layer being deposited at a second deposition rate that is higher than the first deposition rate wherein the gaps have a diameter of less than 0.5 μm.

24. The method of claim 23, wherein the dielectric film comprises silicon oxide, the first and second process gases including a silicon reactant and an oxygen reactant, the second process gas containing higher amounts of the silicon and oxygen reactants than the first process gas.

25. The method of claim 23, wherein the dielectric film comprises silicon oxide, and the first process gas includes a higher amount of the noble gas than the second process gas.

26. The method of claim 23, wherein the RF bias being higher during the gap filling step than during the capping step.

27. The method of claim 23, wherein the substrate is positioned on a substrate holder that is maintained at a temperature of about 80° C. to 200° C.

28. The method of claim 23, wherein the process gas is introduced through a gas supply including orifices, at least some of the orifices orienting the process gas along an axis of injection which intersects an exposed surface of the substrate at an acute angle.

29. A method of depositing a dielectric film substrate comprising the steps of:

providing a substrate in a process chamber of an inductively coupled plasma-enhanced chemical vapor deposition (PECVD) reactor wherein the substrate is positioned on a substrate holder;

introducing a process gas comprising a noble gas into the process chamber wherein the amount of noble gas is sufficient to cause sputter etching;

controlling the temperature on a surface of the substrate holder;

applying a radio frequency bias to the substrate; and

energizing the process gas into a plasma state by inductively coupling RF energy into the process chamber and growing a dielectric film on the substrate by PECVD the dielectric film being deposited in gaps between electrically conductive lines on the substrate wherein the gaps have a diameter of less than 0.5 μm and the dielectric film substantially fills the gaps.

30. The method of claim 29, wherein the process gas further comprises a silicon-containing reactant gas selected from the group consisting of SiH_4, Si_2H_6, SiF_4, TEOS, TMCTS, and mixtures thereof, said process further comprising decomposing the silicon-containing reactant to form a silicon containing gas and plasma phase reacting said silicon-containing gas on a surface of the substrate.

31. The method of claim 30, wherein the process gas comprises a reactant gas selected from the group consisting of H_2, O_2, N_2, NH_3, NF_3, N_2O, and NO, and mixtures thereof.

32. The method of claim 30, wherein the process gas comprises a reactant gas selected from the group consisting of boron-containing gas, phosphorous-containing gas, and mixtures thereof.

33. The method of claim 31, wherein the process gas comprises a reactant gas selected from the group consisting of boron-containing gas, phosphorous-containing gas, and mixtures thereof.

34. The method of claim 29, wherein the process chamber is a vacuum maintained at about 1 mTorr to about 30 mTorr.

35. The method of claim 29, wherein the step of applying a radio frequency bias to the substrate comprises supporting the substrate on a substrate holder having an electrode supplying a radio frequency bias to the substrate, the radio frequency bias being generated by supplying the electrode with at least 2 watts/cm^2 of power.

36. The method of claim 29, wherein the radio frequency bias applied to the substrate is at a frequency of between about 100 kHz to 27 MHz.

37. The method of claim 29, wherein the substrate is positioned on a substrate holder that is maintained at a temperature of about 80° C. to 200° C.

38. The method of claim 37, further comprising supplying a heat transfer gas between a surface of the substrate and a surface of a substrate holder.

39. The method of claim 38, further comprising clamping the substrate on an electrostatic or mechanical chuck during the film growing step.

40. The method of claim 39, wherein the heat transfer gas which comprises helium and/or argon is supplied to a space between a surface of the substrate and a surface of the chuck.

41. The method of claim 37, wherein the dielectric film comprises silicon oxide.

42. The method of claim 37, wherein the dielectric film comprises SiO_2.

43. The method of claim 37, wherein the process gas includes a silicon and fluorine-containing reactants and the dielectric film comprises silicon oxyfluoride.

44. The method of claim 29, wherein the gas mixture includes a nitrogen-containing gas and the dielectric film comprises silicon oxynitride.

45. The method of claim 29, wherein the process gas is introduced through a gas supply including orifices, at least some of the orifices orienting the process gas along an axis of injection which intersects an exposed surface of the substrate at an acute angle.

46. The method of claim 1 wherein the inductively coupled plasma-enhanced chemical vapor deposition reactor comprises:

a plasma processing chamber;

a substrate holder supporting the substrate within said processing chamber wherein the substrate holder is at a temperature of about 80° C. to 200° C.;

an electrically-conductive coil disposed outside said processing chamber;

means for introducing the process gas into said processing chamber; and

an RF energy source which inductively couples RF energy into the processing chamber to energize the process gas into a plasma state.

47. The method of claim 1 wherein the gaps have a diameter of 0.25 μm or less.

48. The method of claim 23 wherein the inductively coupled plasma-enhanced chemical vapor deposition reactor comprises:

a plasma processing chamber;

a substrate holder supporting the substrate within said processing chamber wherein the substrate holder is at a temperature of about 80° C. to 200° C.;

an electrically-conductive coil disposed outside said processing chamber;

means for introducing the process gas into said processing chamber; and

an RF energy source which inductively couples RF energy into the processing chamber to energize the process gas into a plasma state.

49. The method of claim 23, wherein the gaps have a diameter of 0.25 μm or less.

50. The method of claim 29 wherein the inductively coupled plasma-enhanced chemical vapor deposition reactor comprises:

a plasma processing chamber;

a substrate holder supporting the substrate within said processing chamber wherein the substrate holder is at a temperature of about 80° C. to 200° C.;

an electrically-conductive coil disposed outside said processing chamber;

means for introducing the process gas into said processing chamber; and

an RF energy source which inductively couples RF energy into the processing chamber to energize the process gas into a plasma state.

51. The method of claim 29 wherein the gaps have a diameter of 0.25 μm or less.

52. The method of claim 1 wherein the gaps have an aspect ratio of 3:1 or higher.

53. The method of claim 23 wherein the gaps have an aspect ratio of 3:1 or higher.

54. The method of claim 29 wherein the gaps have an aspect ratio of 3:1 or higher.

55. The method of claim 1 wherein the gaps have a diameter that is between less than 0.5 μm to 0.25 μm and have an aspect ratio of 3:1 or higher.

56. The method of claim 23 wherein the gaps have a diameter that is between less than 0.5 μm to 0.25 μm and have an aspect ratio of 3:1 or higher.

57. The method of claim 29 wherein the gaps have a diameter that is between less than 0.5 μm to 0.25 μm and have an aspect ratio of 3:1 or higher.

58. The method of claim 1 wherein the gaps that are filled are void-free.

59. The method of claim 23 wherein the gaps that are filled are void-free.

60. The method of claim 29 wherein the gaps that are filled are void-free.

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